FIG. 1

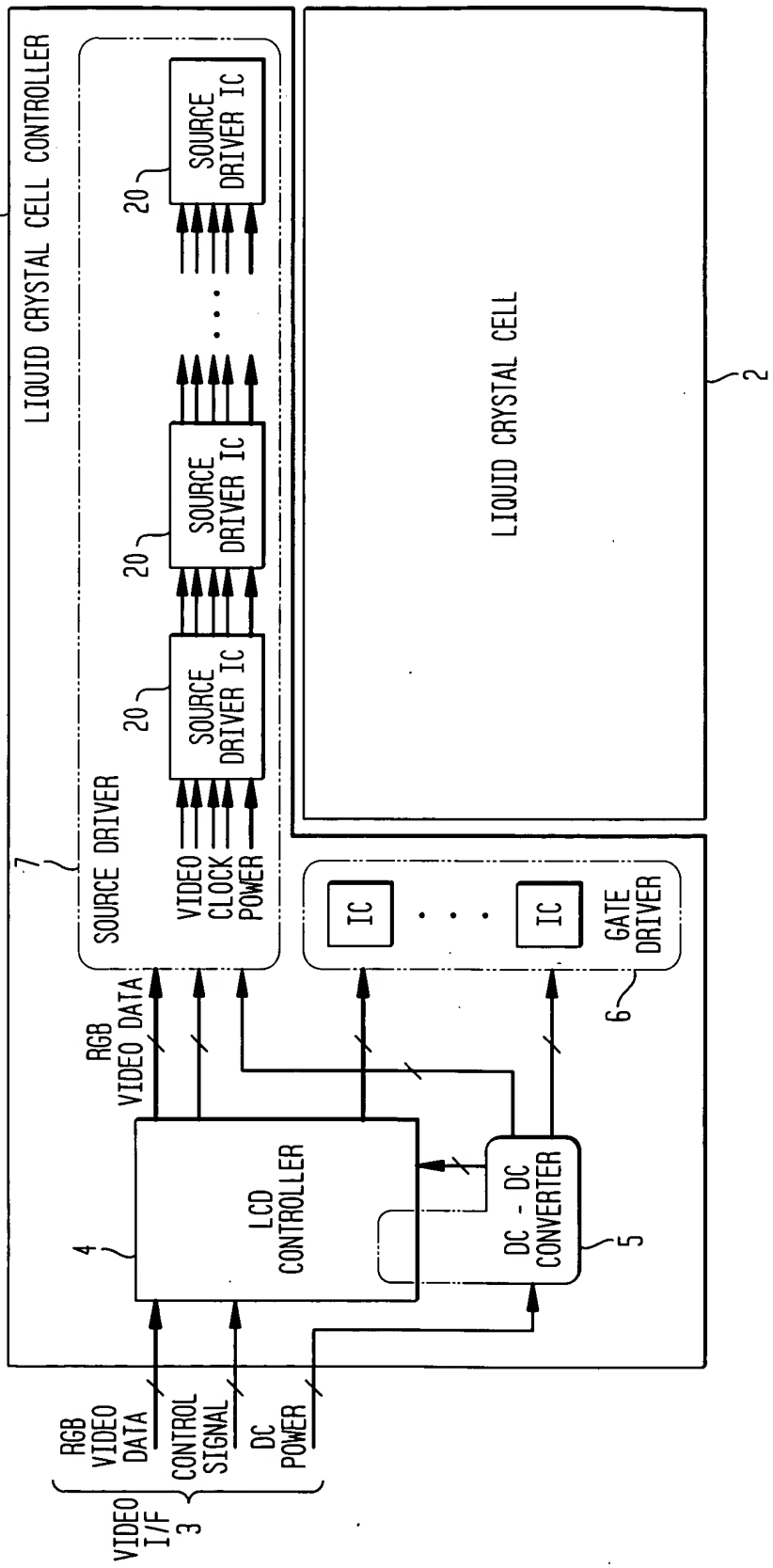

LIQUID CRYSTAL CELL CONTROLLER
1
LIQUID CRYSTAL CELL
2
VIDEO I/F
3
RGB VIDEO DATA
CONTROL SIGNAL
DC POWER
4
LCD CONTROLLER
5
DC - DC CONVERTER
6
GATE DRIVER
IC
IC
7
SOURCE DRIVER
VIDEO
CLOCK
POWER
20
SOURCE DRIVER IC
20
SOURCE DRIVER IC
20
SOURCE DRIVER IC
RGB VIDEO DATA

FIG. 2

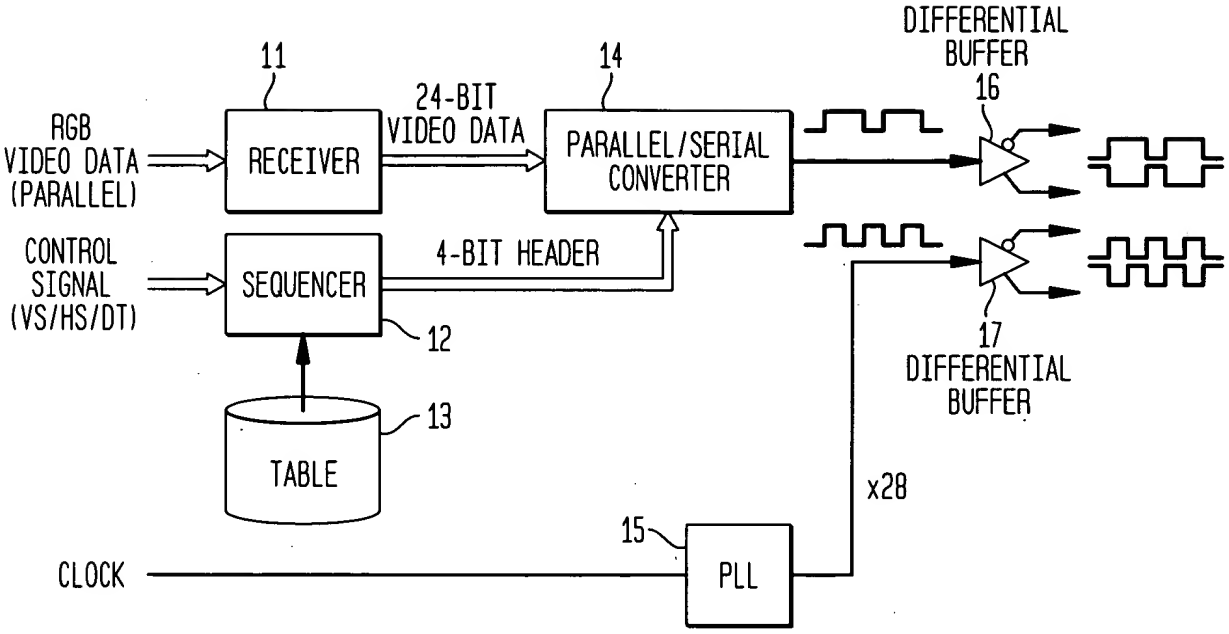

11
14
DIFFERENTIAL BUFFER
16
RGB VIDEO DATA (PARALLEL)
RECEIVER
24-BIT VIDEO DATA
PARALLEL/SERIAL CONVERTER
CONTROL SIGNAL (VS/HS/DT)
SEQUENCER
4-BIT HEADER
12
17
DIFFERENTIAL BUFFER
13
TABLE
x28
15
CLOCK
PLL

FIG. 3

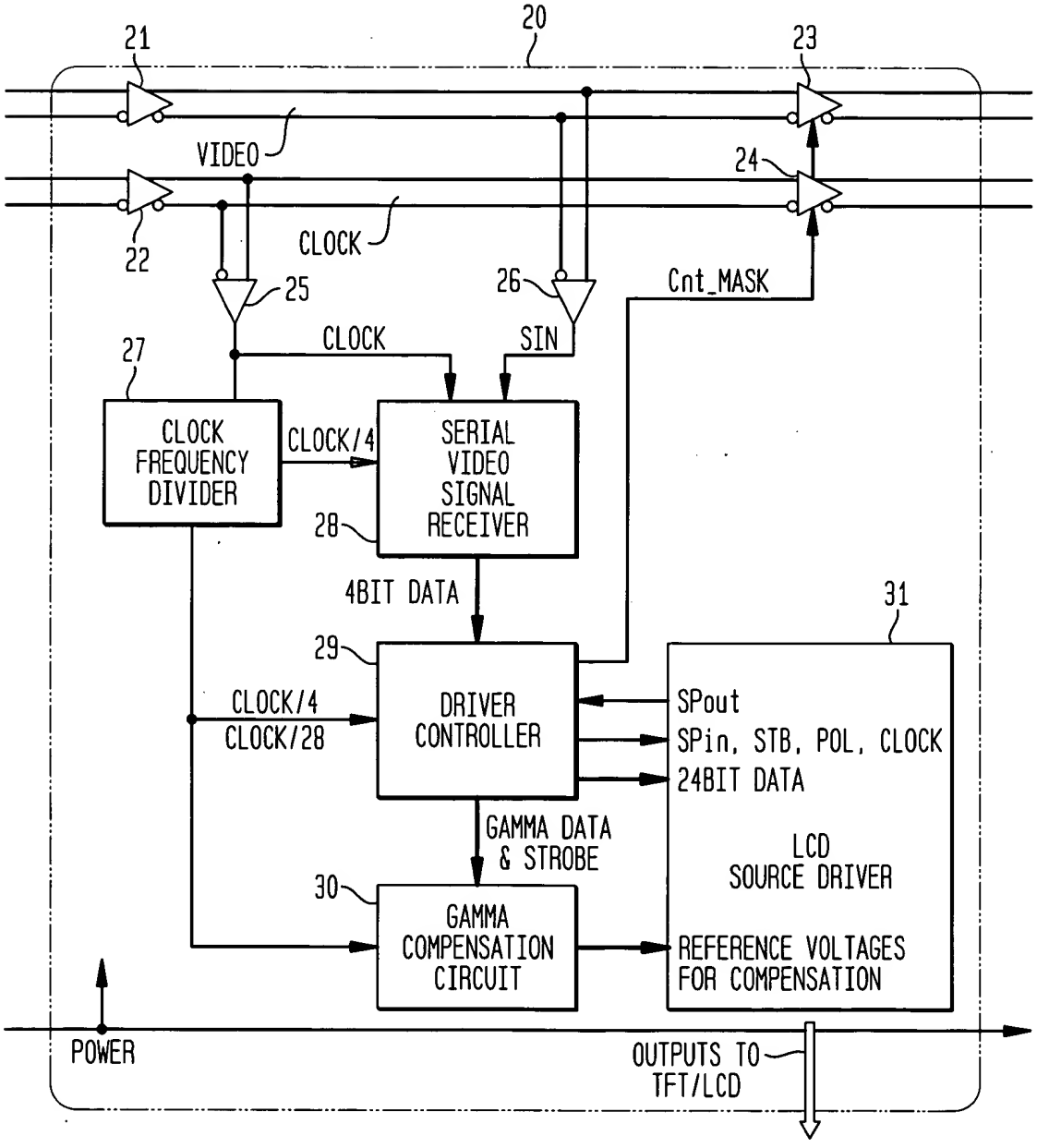

20
21
23
VIDEO
24
22
CLOCK
25
26
Cnt_MASK
CLOCK
SIN
27
CLOCK FREQUENCY DIVIDER
CLOCK/4
SERIAL VIDEO SIGNAL RECEIVER
28
4BIT DATA
31
29
CLOCK/4
CLOCK/28
DRIVER CONTROLLER
SPout
SPin, STB, POL, CLOCK
24BIT DATA
GAMMA DATA & STROBE
LCD SOURCE DRIVER
30
GAMMA COMPENSATION CIRCUIT
REFERENCE VOLTAGES FOR COMPENSATION
POWER
OUTPUTS TO TFT/LCD

FIG. 4

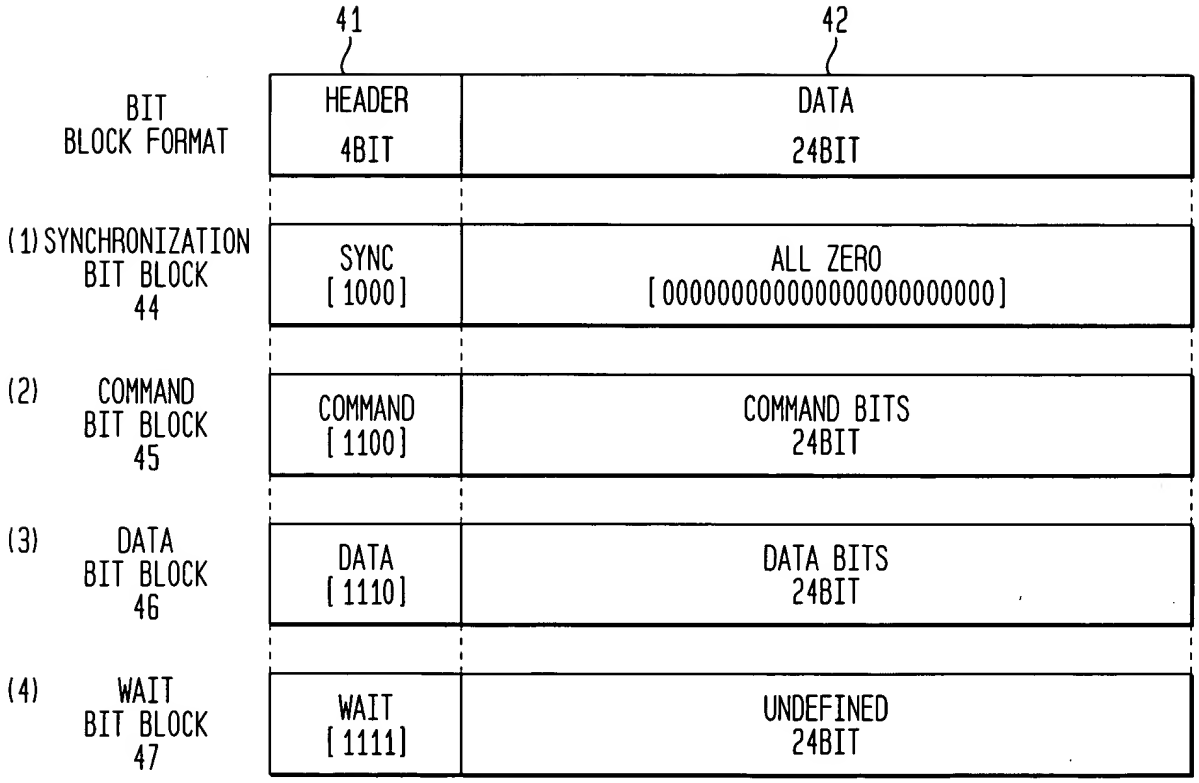

41
42
BIT
BLOCK FORMAT
HEADER
4BIT
DATA
24BIT
(1) SYNCHRONIZATION
BIT BLOCK
44
SYNC
[1000]
ALL ZERO
[000000000000000000000000]
(2) COMMAND
BIT BLOCK
45
COMMAND
[1100]
COMMAND BITS
24BIT
(3) DATA
BIT BLOCK
46
DATA
[1110]
DATA BITS
24BIT
(4) WAIT
BIT BLOCK
47
WAIT
[1111]
UNDEFINED
24BIT

FIG. 5A

INITIAL SETUP

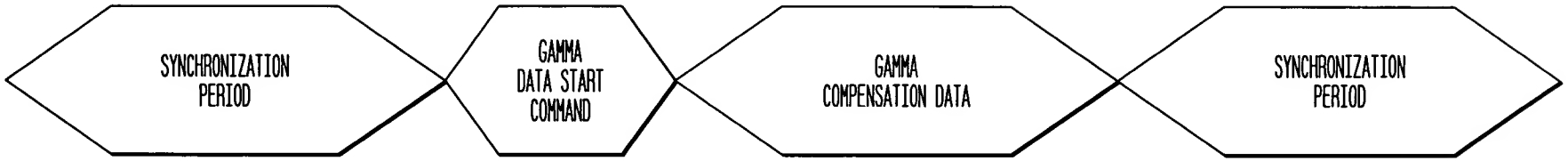


FIG. 5B

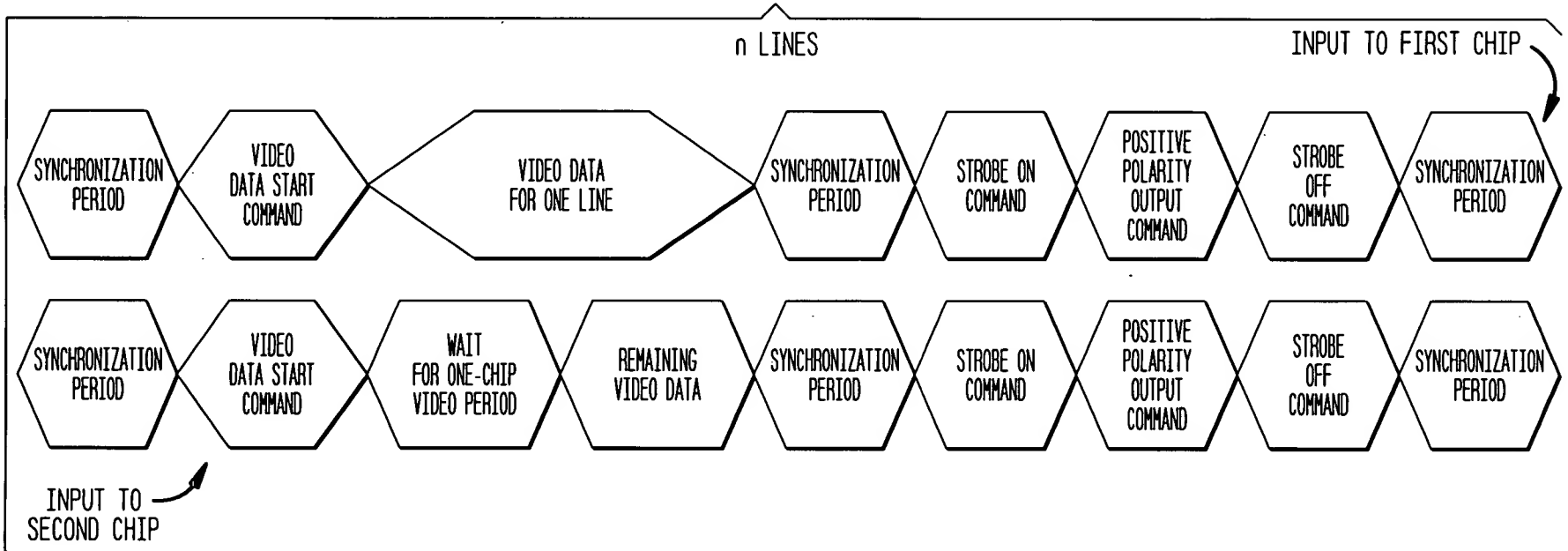


FIG. 5C

n+1 LINES

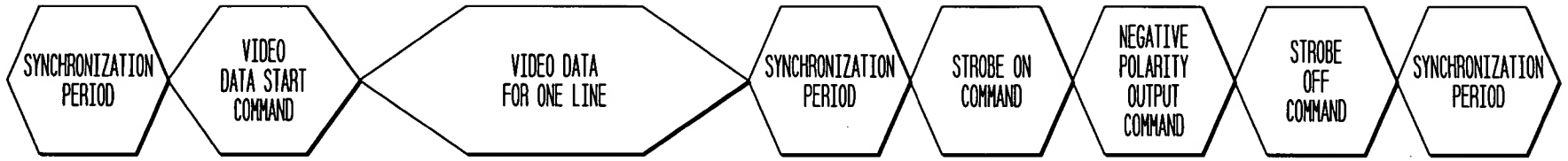


FIG. 6

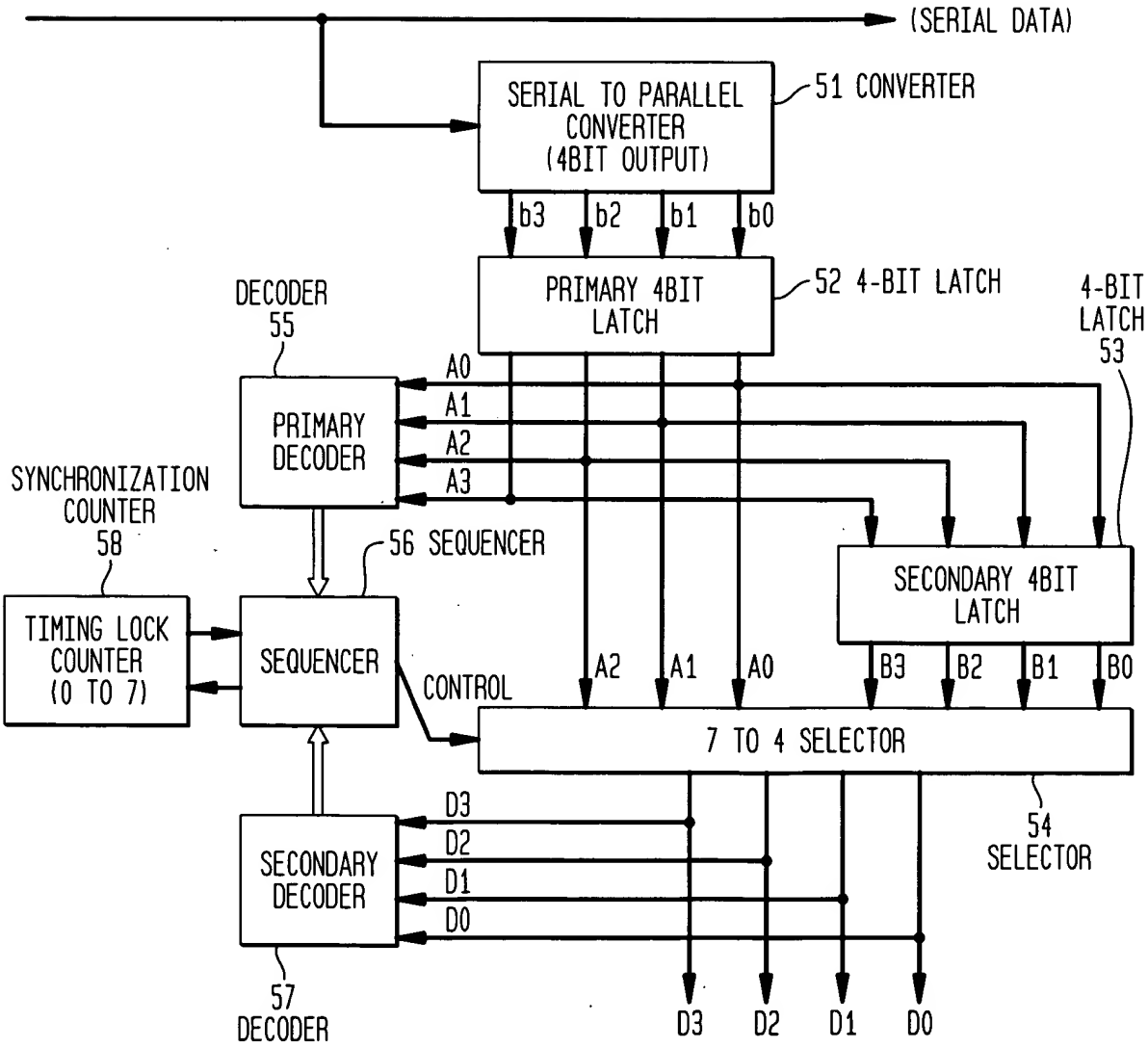

(SERIAL DATA)
SERIAL TO PARALLEL CONVERTER (4BIT OUTPUT)
51 CONVERTER
b3
b2
b1
b0
PRIMARY 4BIT LATCH
52 4-BIT LATCH
4-BIT LATCH 53
DECODER 55
PRIMARY DECODER
A0
A1
A2
A3
SYNCHRONIZATION COUNTER 58
56 SEQUENCER
SECONDARY 4BIT LATCH
TIMING LOCK COUNTER (0 TO 7)
SEQUENCER
CONTROL
A2
A1
A0
B3
B2
B1
B0
7 TO 4 SELECTOR
54 SELECTOR
D3
D2
D1
D0
SECONDARY DECODER
57 DECODER
D3
D2
D1
D0

FIG. 7

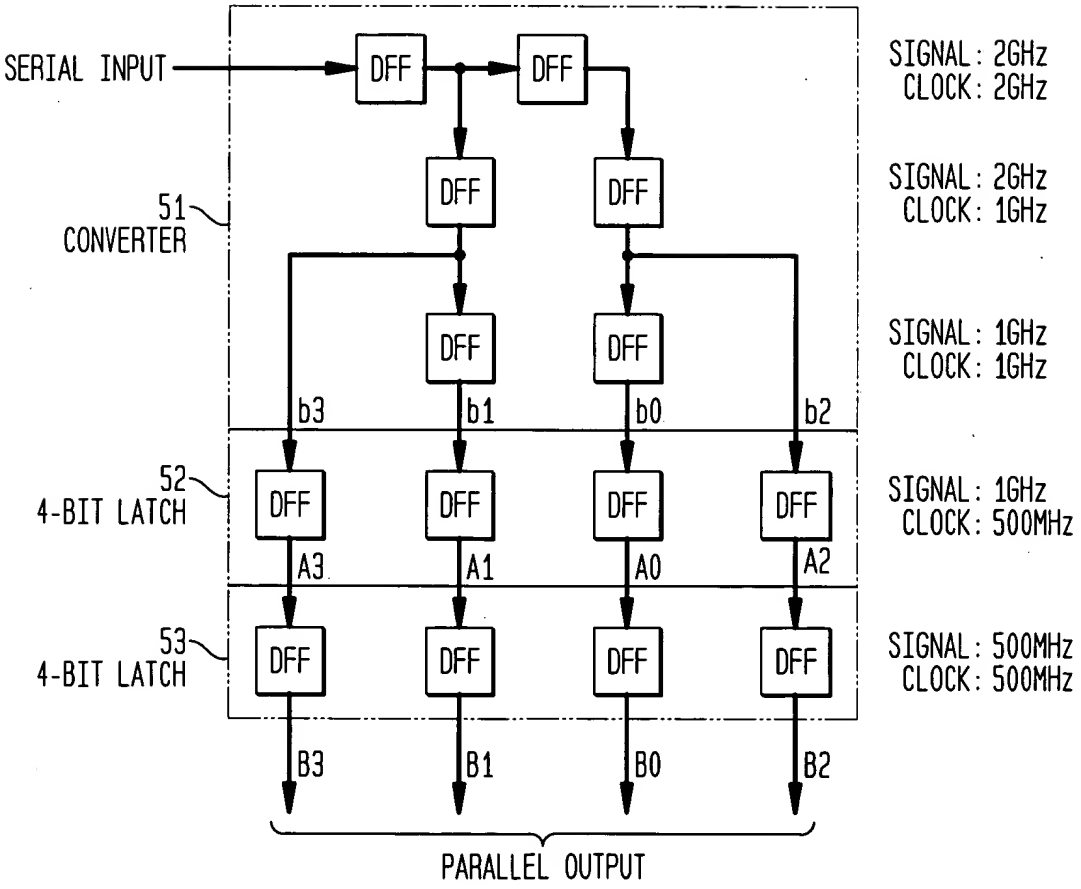

SERIAL INPUT
DFF
DFF
DFF
DFF
DFF
DFF
51
CONVERTER
b3
b1
b0
b2
52
4-BIT LATCH
DFF
DFF
DFF
DFF
A3
A1
A0
A2
53
4-BIT LATCH
DFF
DFF
DFF
DFF
B3
B1
B0
B2
PARALLEL OUTPUT
SIGNAL: 2GHz
CLOCK: 2GHz
SIGNAL: 2GHz
CLOCK: 1GHz
SIGNAL: 1GHz
CLOCK: 1GHz
SIGNAL: 1GHz
CLOCK: 500MHz
SIGNAL: 500MHz
CLOCK: 500MHz

FIG. 8

4-BIT LATCH (n CLOCK) [A3, A2, A1, A0]	SELECTOR (n+1 CLOCK) [D3, D2, D1, D0]	CONTROL ID
[1, 0, 0, 0]	[A2, A1, A0, B3]	0
[0, 1, 0, 0]	[A1, A0, B3, B2]	1
[0, 0, 1, 0]	[A0, B3, B2, B1]	2
[0, 0, 0, 1]	[B3, B2, B1, B0]	3

FIG. 9

BIT BLOCK TYPE	COMPARISON PATTERN WITH SELECTOR OUTPUT [D3, D2, D1, D0]
SYNCHRONIZATION	[0, 0, 0, 1]
COMMAND	[0, 0, 1, 1]
DATA	[0, 1, 1, 1]
WAIT	[1, 1, 1, 1]

FIG. 10

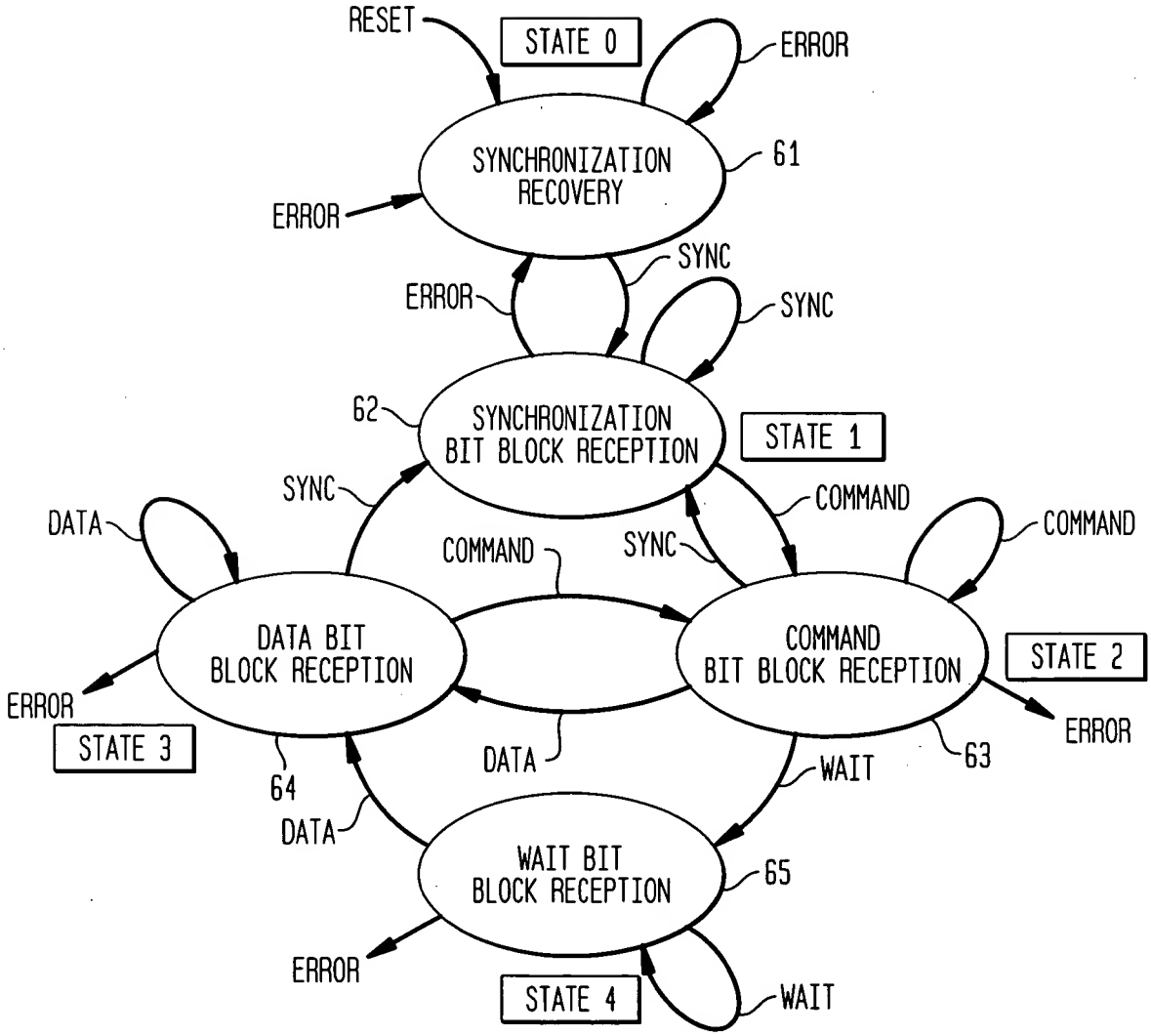

RESET
STATE 0
ERROR
SYNCHRONIZATION
RECOVERY
61
ERROR
ERROR
SYNC
SYNC
62
SYNCHRONIZATION
BIT BLOCK RECEPTION
STATE 1
SYNC
COMMAND
COMMAND
DATA
COMMAND
SYNC
DATA BIT
BLOCK RECEPTION
COMMAND
BIT BLOCK RECEPTION
STATE 2
ERROR
STATE 3
ERROR
DATA
WAIT
63
64
DATA
WAIT BIT
BLOCK RECEPTION
65
ERROR
STATE 4
WAIT

FIG. 11

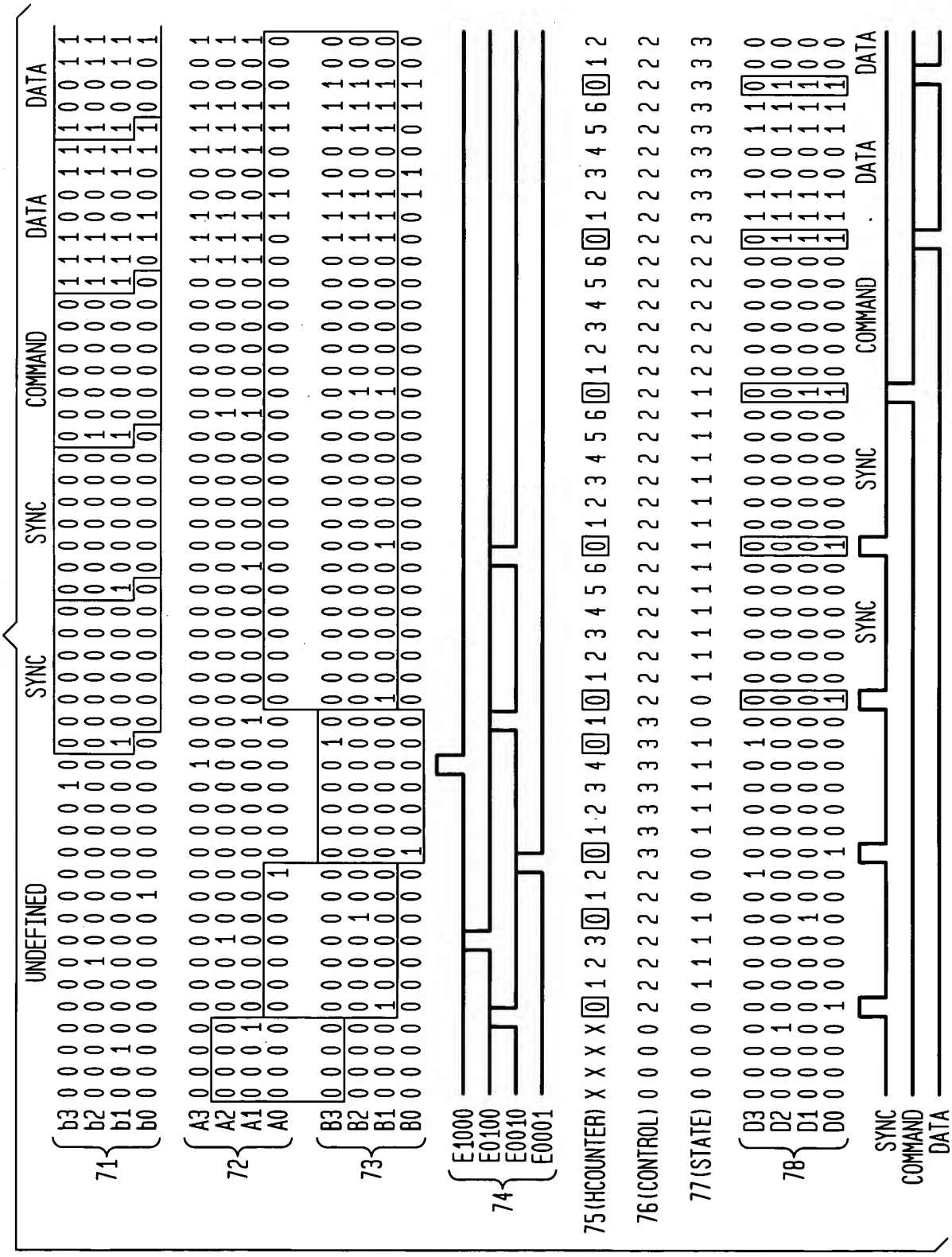

UNDEFINED
SYNC
COMMAND
DATA
71
b3
b2
b1
b0
72
A3
A2
A1
A0
73
B3
B2
B1
B0
74
E1000
E0100
E0010
E0001
75(HCOUNTER)
76(CONTROL)
77(STATE)
78
D3
D2
D1
D0
SYNC
COMMAND
DATA

FIG. 12

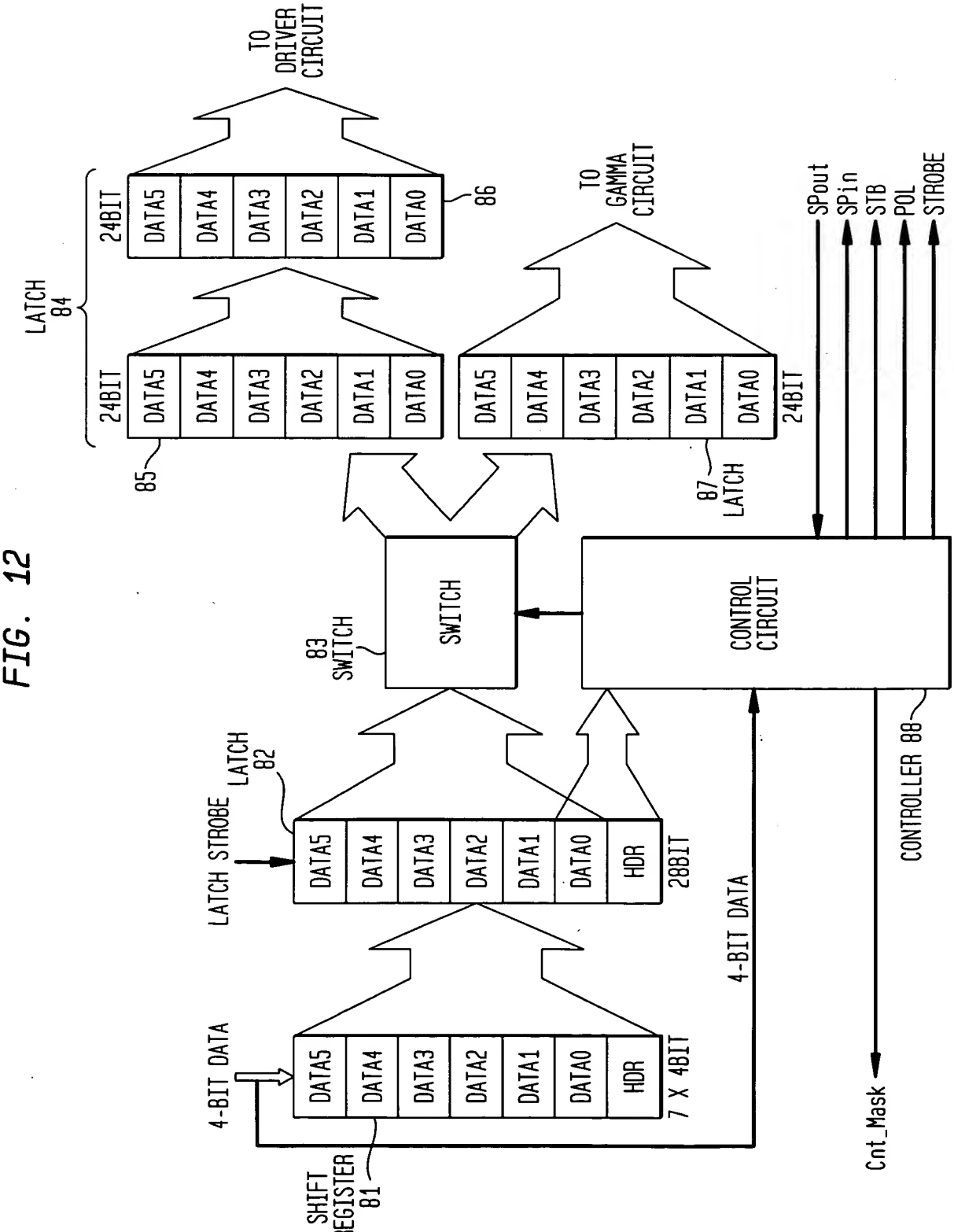

TO DRIVER CIRCUIT
TO GAMMA CIRCUIT
LATCH 84
24BIT
DATA5
DATA4
DATA3
DATA2
DATA1
DATA0
86
85
87
LATCH
SPout
SPin
STB
POL
STROBE
SWITCH
83 SWITCH
CONTROL CIRCUIT
LATCH 82
LATCH STROBE
HDR
28BIT
4-BIT DATA
CONTROLLER 88
7 X 4BIT
SHIFT REGISTER 81
Cnt_Mask

FIG. 13A

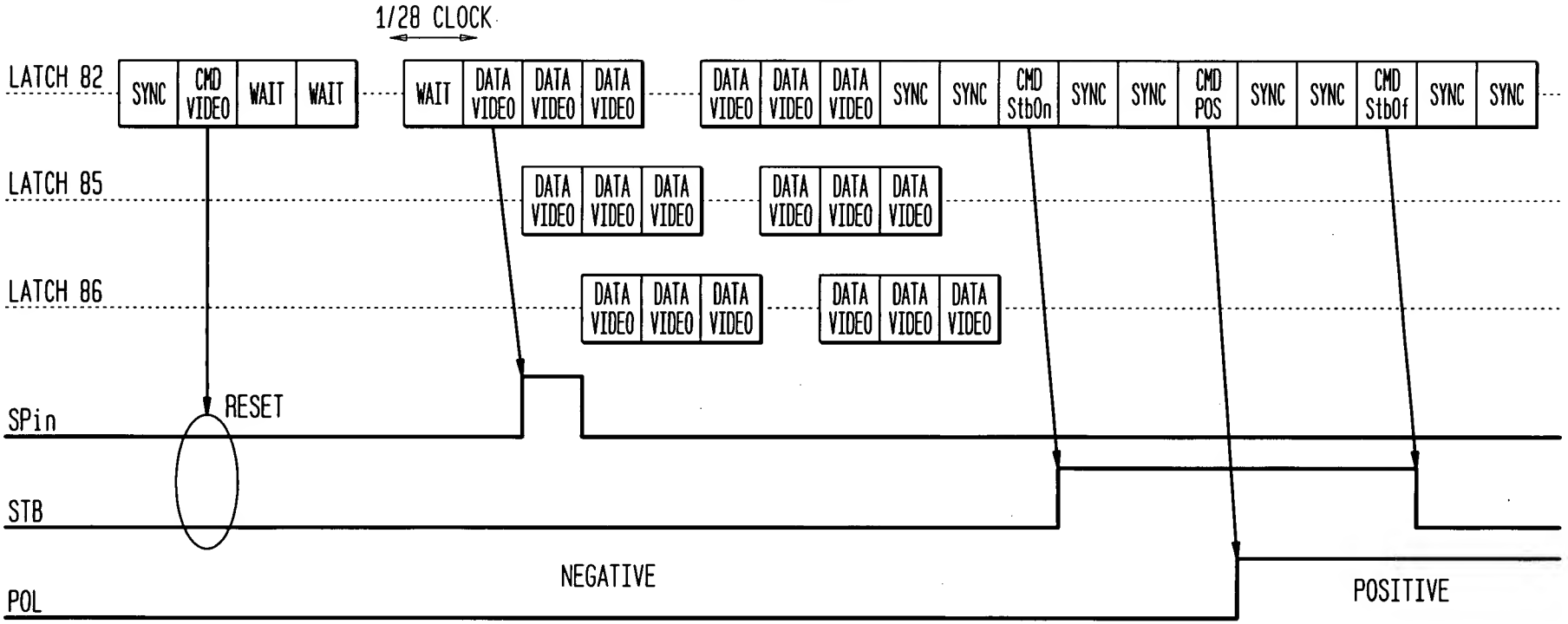


FIG. 13B

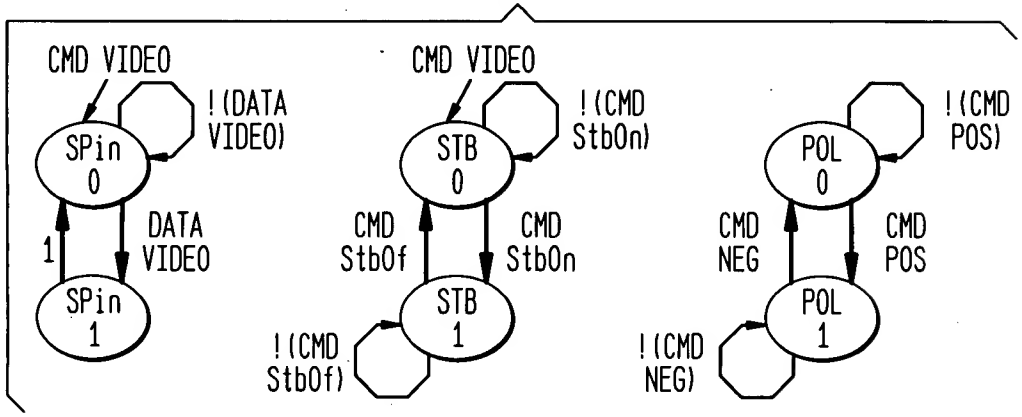


FIG. 14

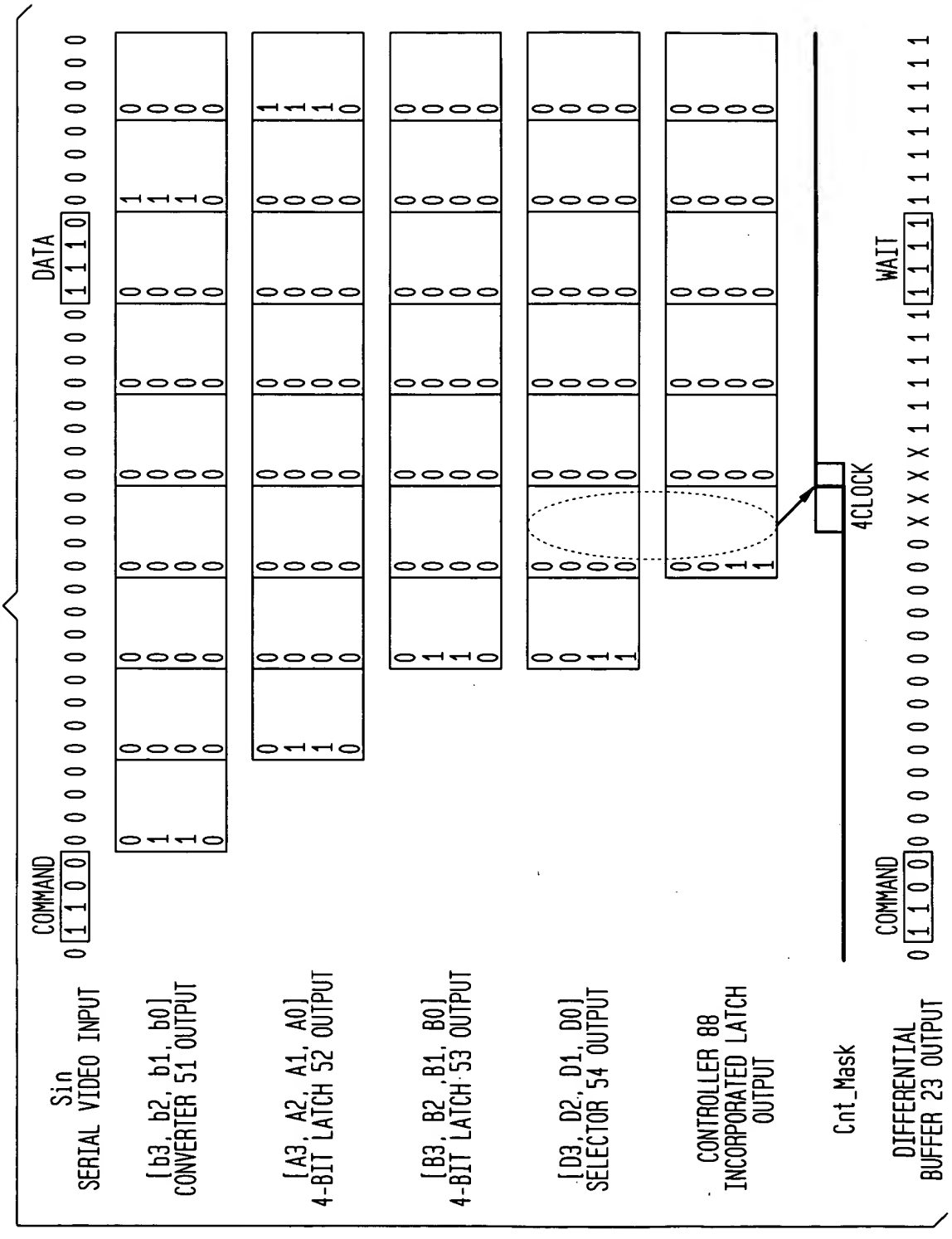

Sin
SERIAL VIDEO INPUT
COMMAND
DATA
[b3, b2, b1, b0]
CONVERTER 51 OUTPUT
[A3, A2, A1, A0]
4-BIT LATCH 52 OUTPUT
[B3, B2, B1, B0]
4-BIT LATCH 53 OUTPUT
[D3, D2, D1, D0]
SELECTOR 54 OUTPUT
CONTROLLER 88
INCORPORATED LATCH
OUTPUT
Cnt_Mask
DIFFERENTIAL
BUFFER 23 OUTPUT
4CLOCK
WAIT

FIG. 15

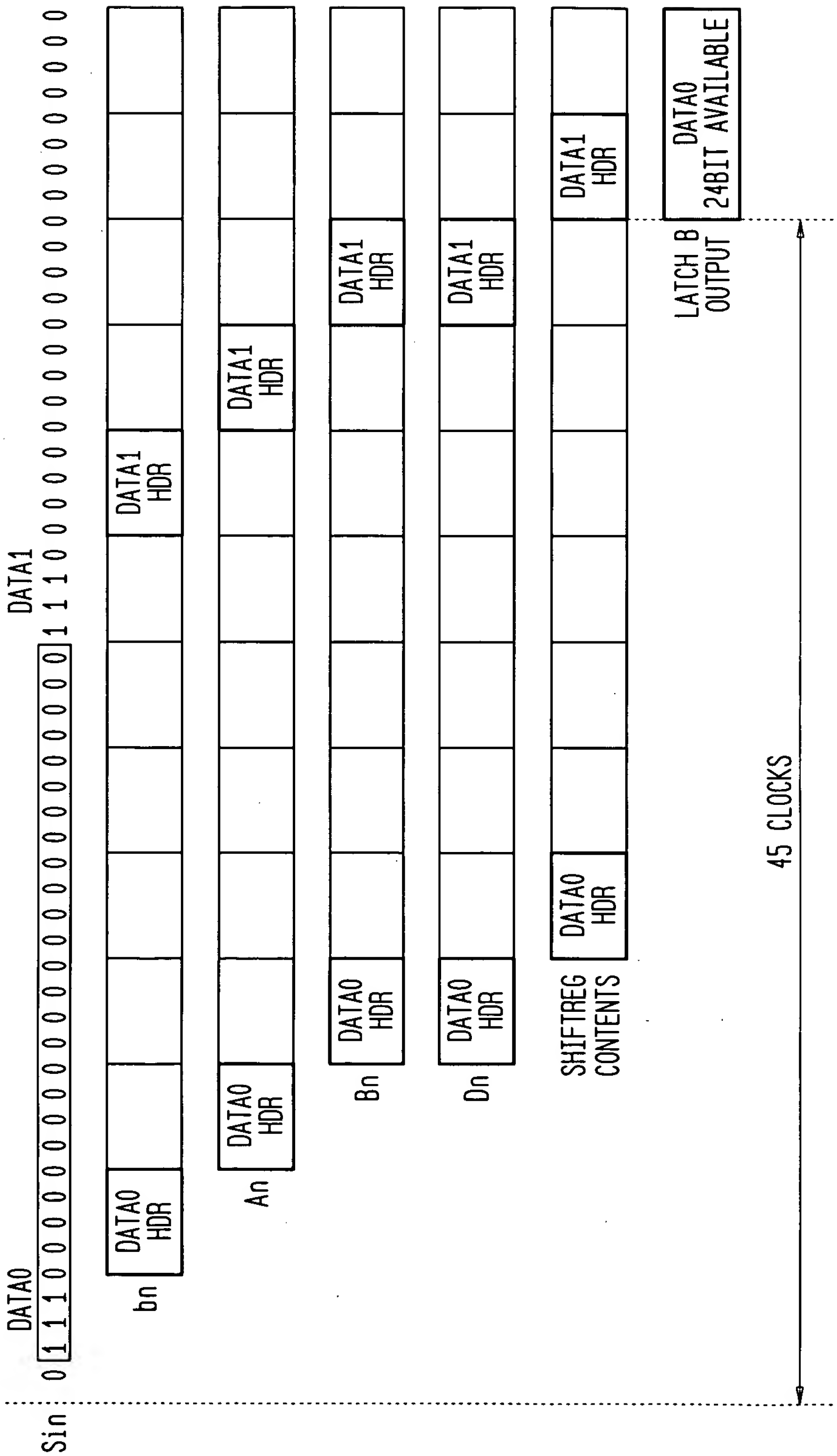

Sin
DATA0
DATA1
bn
An
Bn
Dn
SHIFTREG CONTENTS
DATA0 HDR
DATA1 HDR
LATCH B OUTPUT
DATA0 24BIT AVAILABLE
45 CLOCKS

FIG. 16

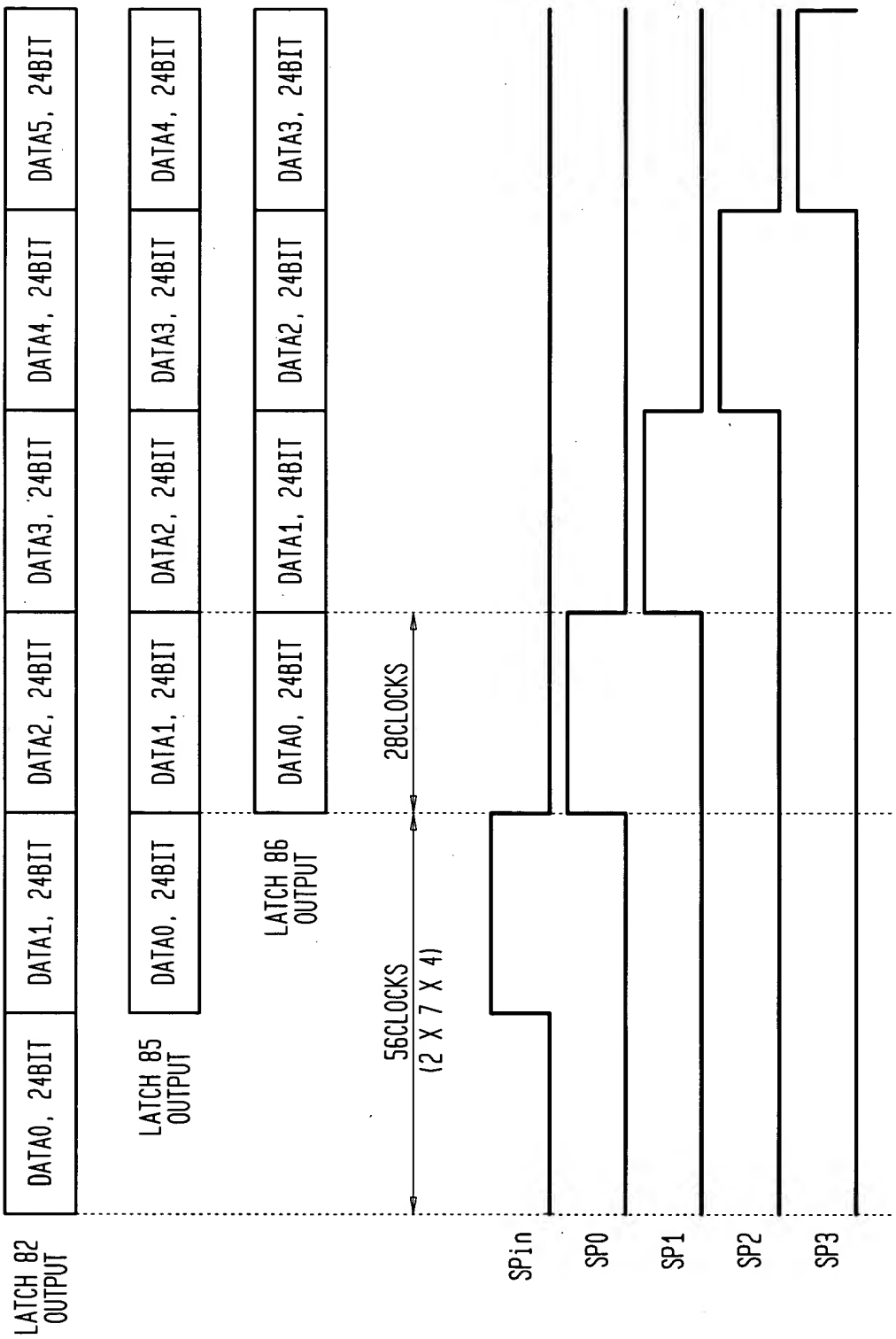

LATCH 82 OUTPUT
DATA0, 24BIT
DATA1, 24BIT
DATA2, 24BIT
DATA3, 24BIT
DATA4, 24BIT
DATA5, 24BIT
LATCH 85 OUTPUT
DATA0, 24BIT
DATA1, 24BIT
DATA2, 24BIT
DATA3, 24BIT
DATA4, 24BIT
LATCH 86 OUTPUT
DATA0, 24BIT
DATA1, 24BIT
DATA2, 24BIT
DATA3, 24BIT
56CLOCKS
(2 X 7 X 4)
28CLOCKS
SPin
SP0
SP1
SP2
SP3

FIG. 17

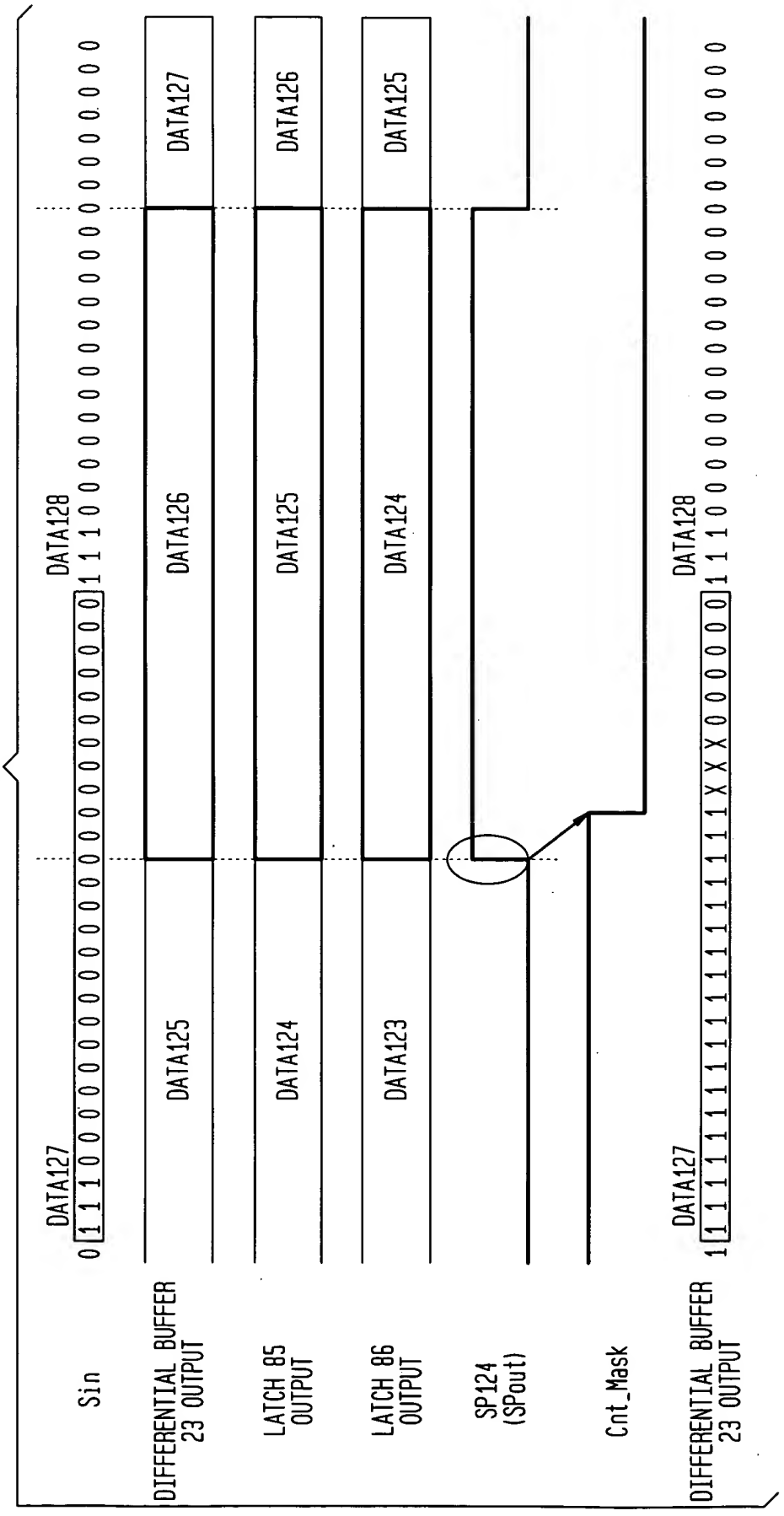

Sin
DIFFERENTIAL BUFFER 23 OUTPUT
LATCH 85 OUTPUT
LATCH 86 OUTPUT
SP124 (SPout)
Cnt_Mask
DIFFERENTIAL BUFFER 23 OUTPUT
DATA127
DATA128
DATA125
DATA126
DATA124
DATA123
0 1 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
1 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 X X X 0 0 0 0 0 0 0 0 0 0 0 0 0 0
1 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

FIG. 18

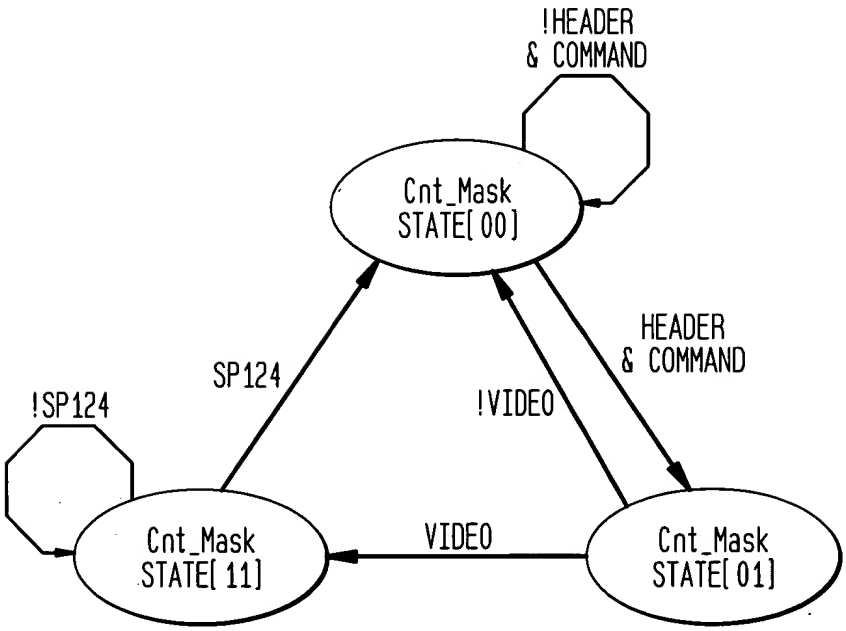

!HEADER
& COMMAND
Cnt_Mask
STATE[00]
HEADER
& COMMAND
SP124
!VIDEO
!SP124
Cnt_Mask
STATE[11]
VIDEO
Cnt_Mask
STATE[01]

FIG. 19

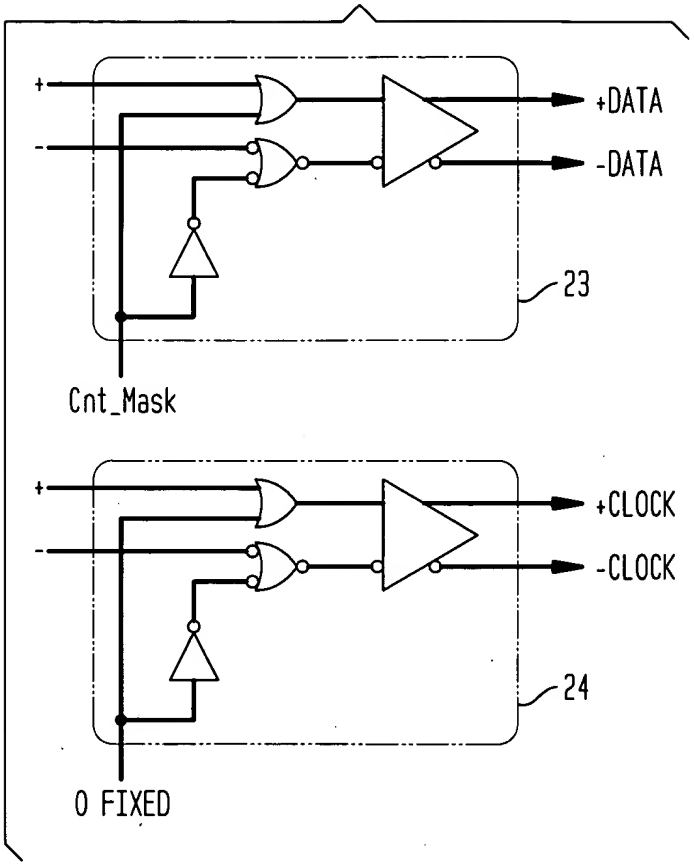
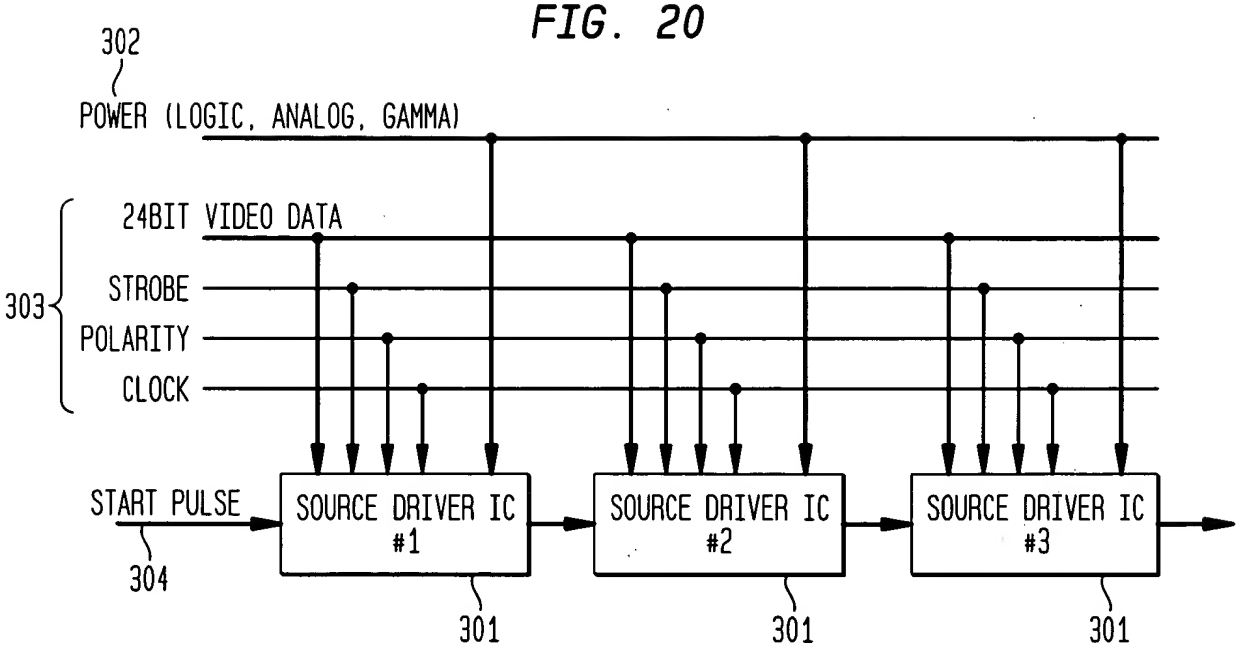


FIG. 20


302
POWER (LOGIC, ANALOG, GAMMA)
24BIT VIDEO DATA
303
STROBE
POLARITY
CLOCK
START PULSE
304
SOURCE DRIVER IC #1
SOURCE DRIVER IC #2
SOURCE DRIVER IC #3
301
301
301

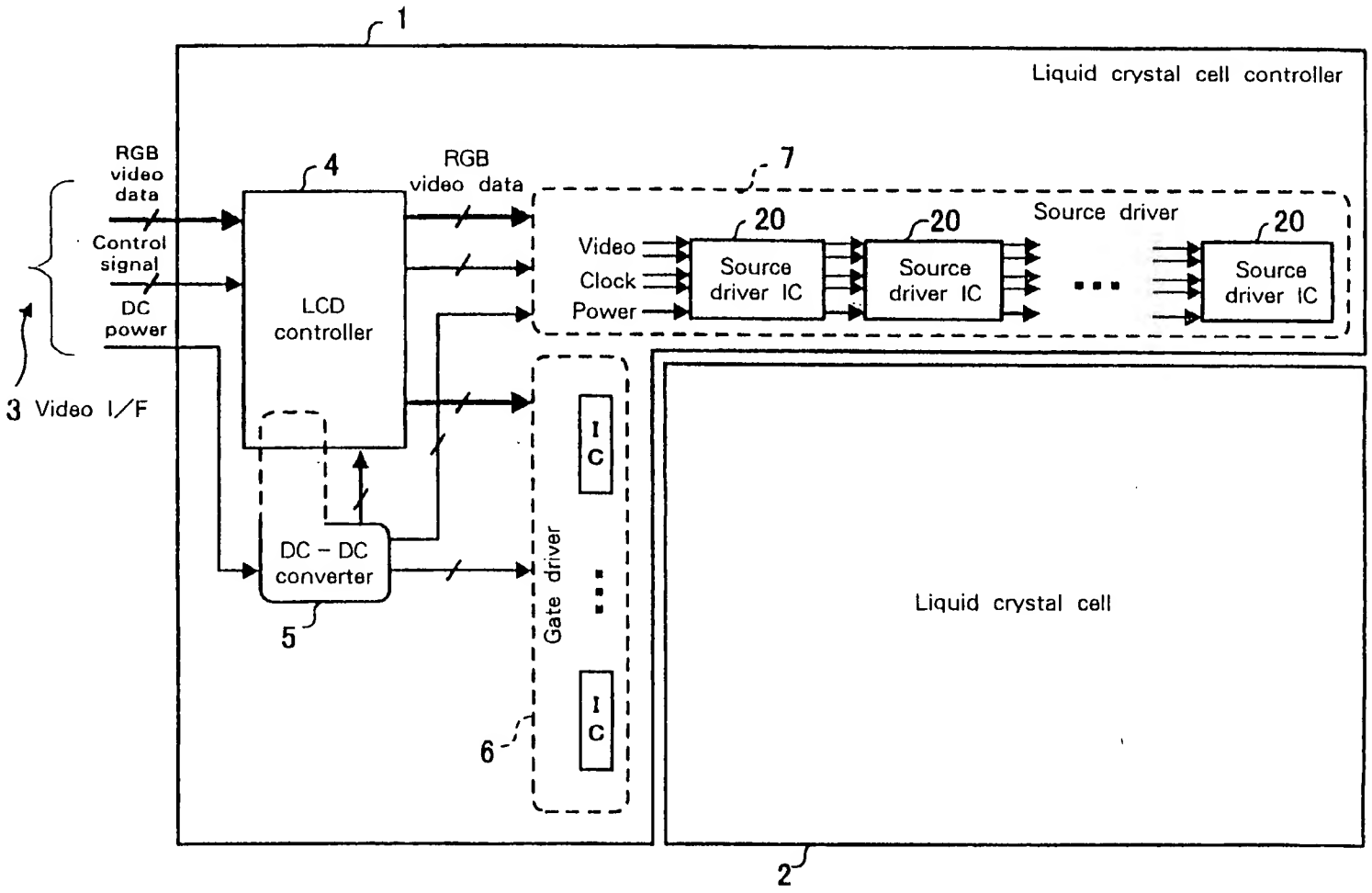

1
Liquid crystal cell controller
RGB video data
Control signal
DC power
3 Video I/F
4
LCD controller
RGB video data
7
Source driver
20
Source driver IC
20
Source driver IC
20
Source driver IC
Video
Clock
Power
DC – DC converter
5
Gate driver
I C
I C
6
Liquid crystal cell
2

Fig. 1

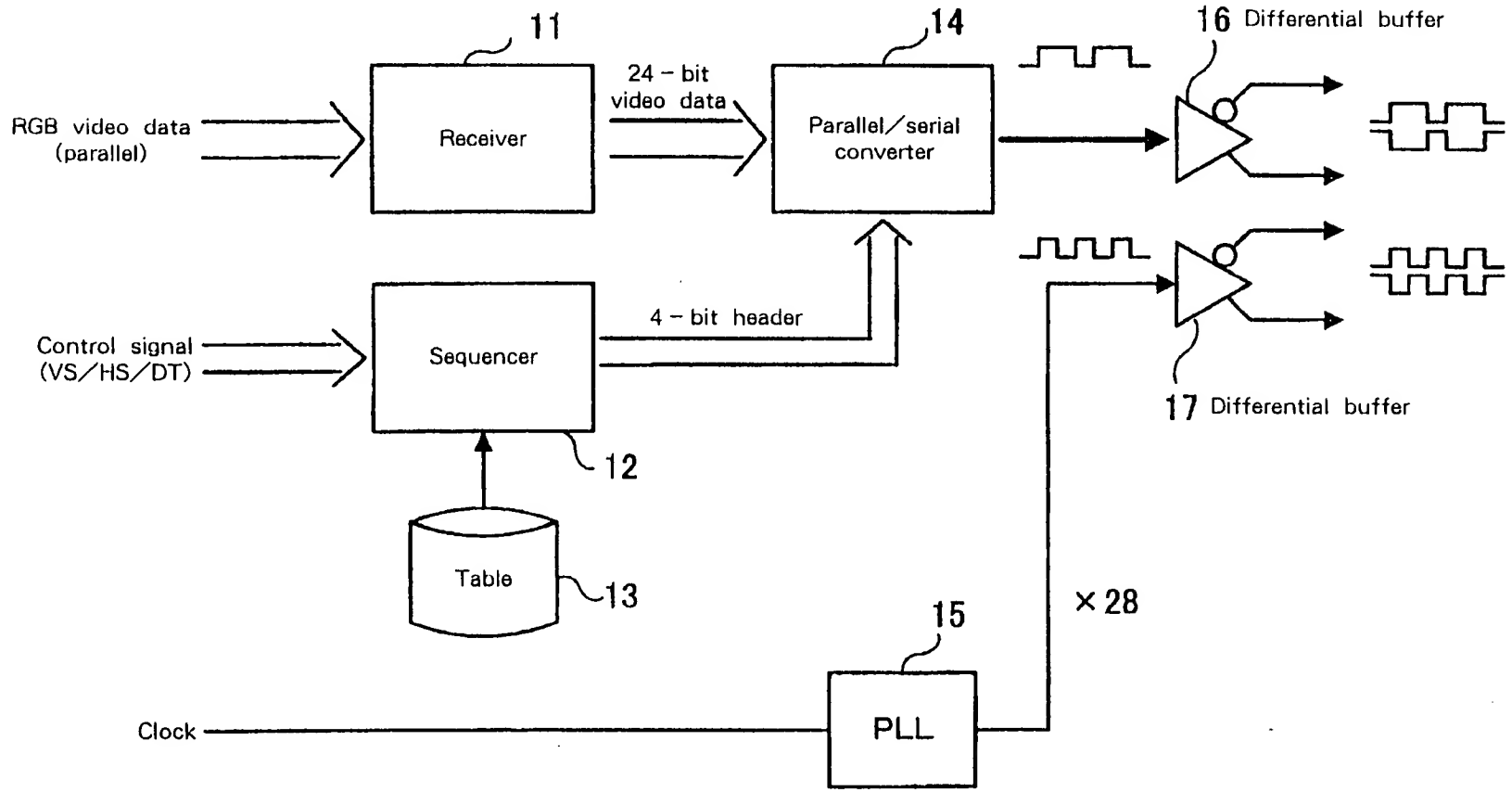

11
14
16 Differential buffer
RGB video data
(parallel)
Receiver
24 – bit
video data
Parallel/serial
converter
Control signal
(VS/HS/DT)
Sequencer
4 – bit header
17 Differential buffer
12
Table
13
15
× 28
Clock
PLL

Fig. 2

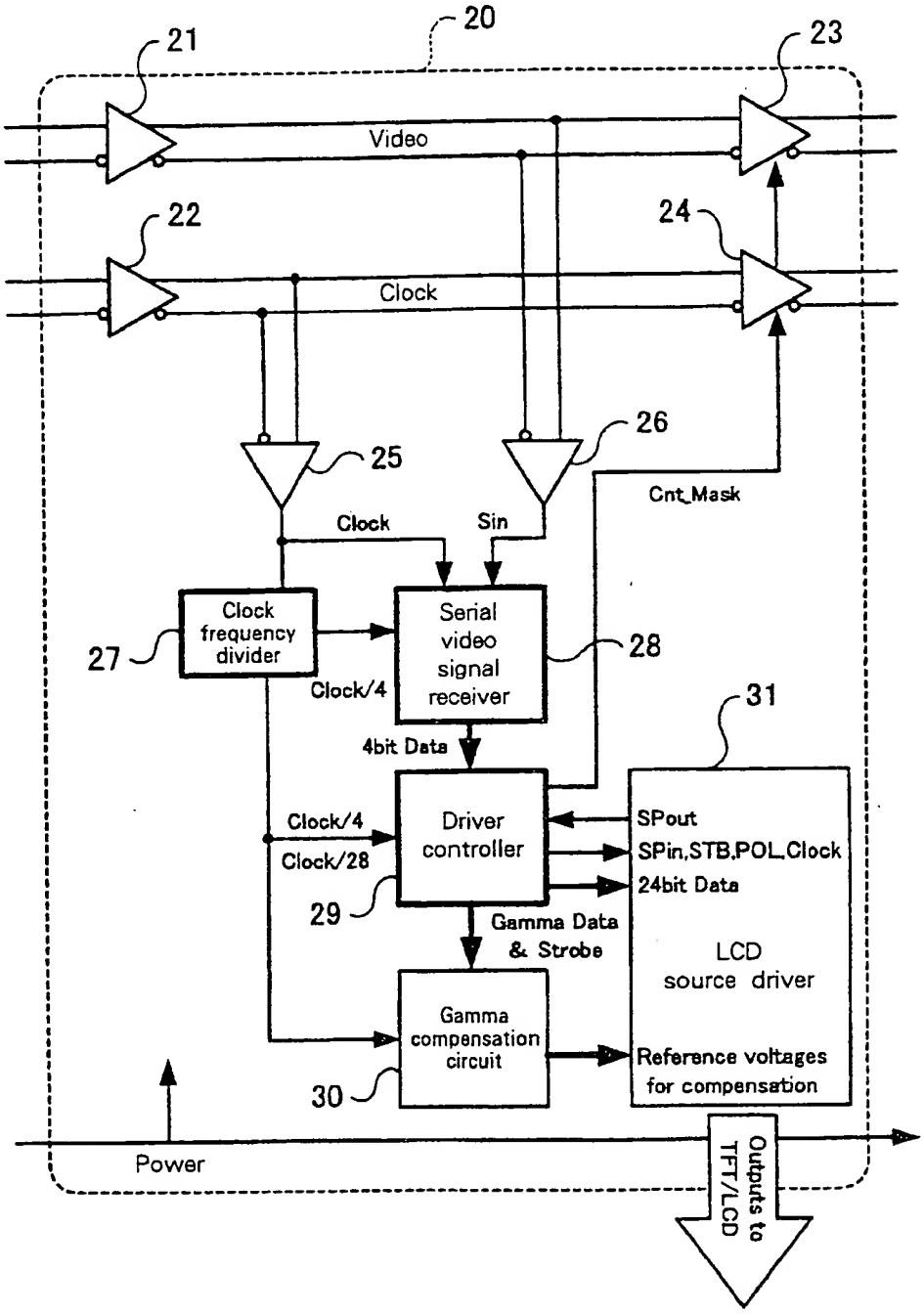

20
21
23
Video
22
24
Clock
25
26
Cnt_Mask
Clock
Sin
Clock frequency divider
27
Clock/4
Serial video signal receiver
28
31
4bit Data
Clock/4
Clock/28
Driver controller
SPout
SPin,STB,POL,Clock
24bit Data
29
Gamma Data & Strobe
LCD source driver
Gamma compensation circuit
Reference voltages for compensation
30
Power
Outputs to TFT/LCD

Fig. 3

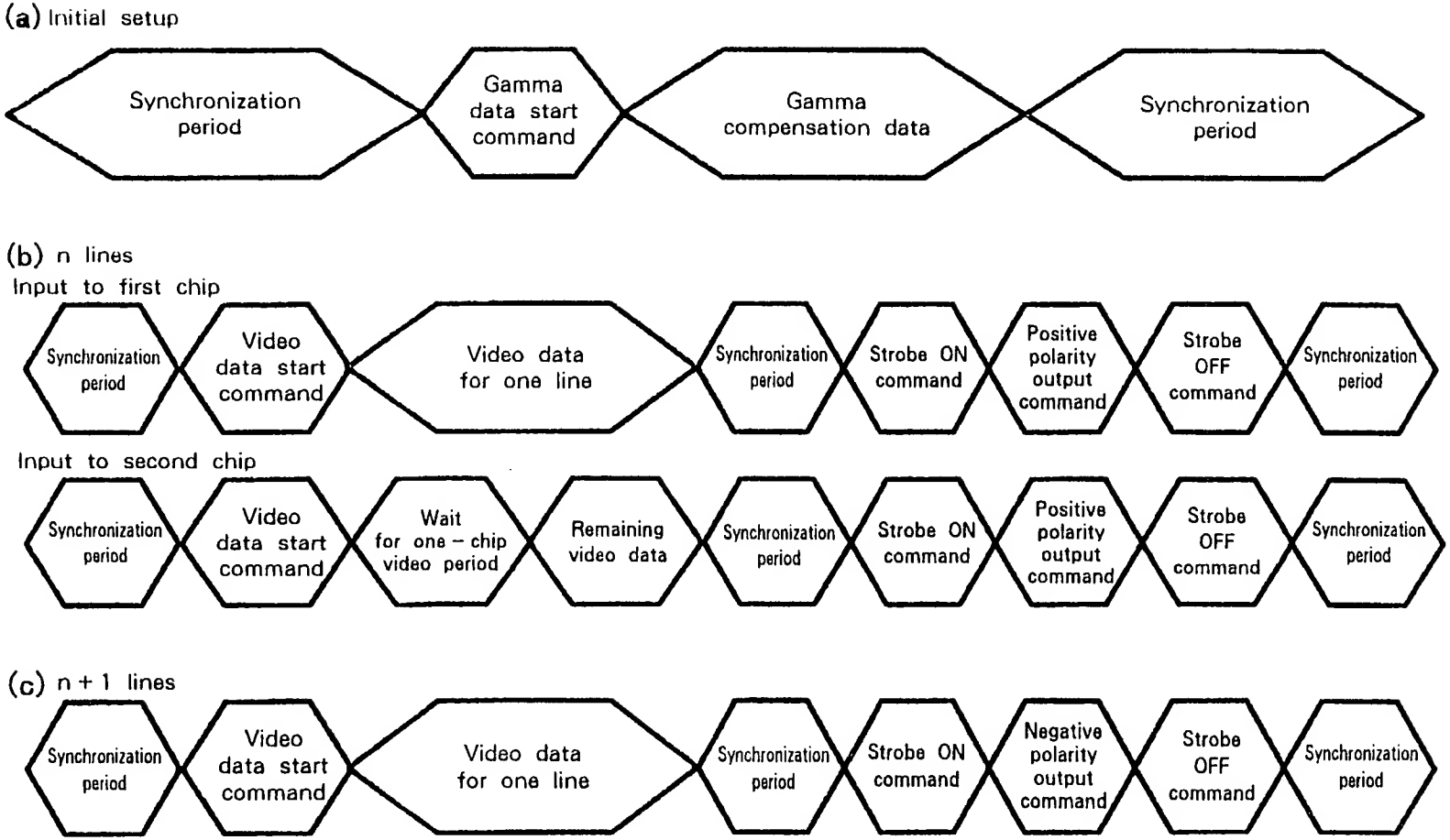

(a) Initial setup
Synchronization period
Gamma data start command
Gamma compensation data
Synchronization period
(b) n lines
Input to first chip
Synchronization period
Video data start command
Video data for one line
Synchronization period
Strobe ON command
Positive polarity output command
Strobe OFF command
Synchronization period
Input to second chip
Synchronization period
Video data start command
Wait for one – chip video period
Remaining video data
Synchronization period
Strobe ON command
Positive polarity output command
Strobe OFF command
Synchronization period
(c) n + 1 lines
Synchronization period
Video data start command
Video data for one line
Synchronization period
Strobe ON command
Negative polarity output command
Strobe OFF command
Synchronization period

Fig. 5

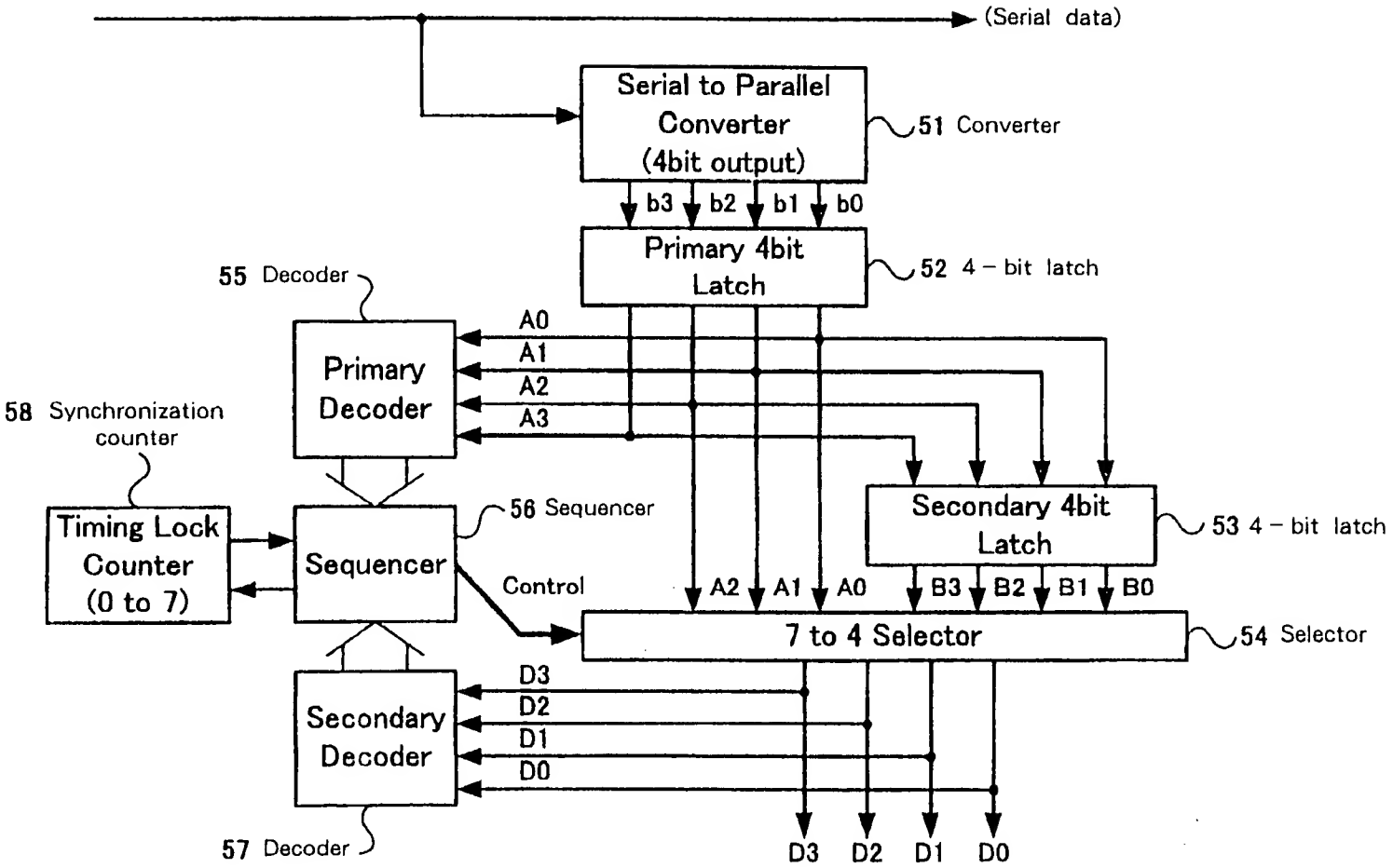

(Serial data)
Serial to Parallel Converter (4bit output)
51 Converter
b3 b2 b1 b0
Primary 4bit Latch
52 4 – bit latch
55 Decoder
Primary Decoder
A0
A1
A2
A3
58 Synchronization counter
Timing Lock Counter (0 to 7)
Sequencer
56 Sequencer
Control
Secondary 4bit Latch
53 4 – bit latch
A2 A1 A0
B3 B2 B1 B0
7 to 4 Selector
54 Selector
Secondary Decoder
D3
D2
D1
D0
57 Decoder
D3 D2 D1 D0

Fig. 6

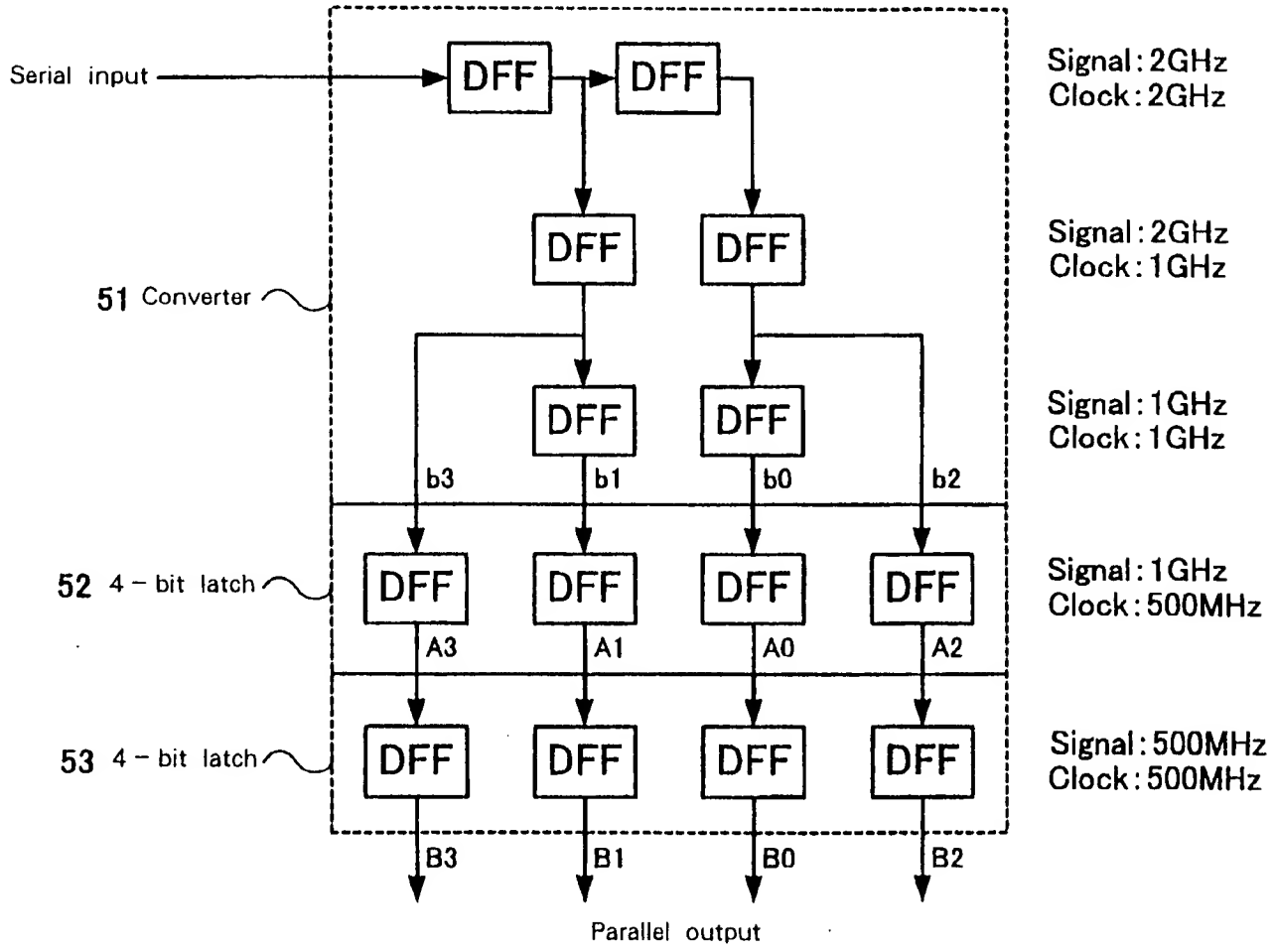

Serial input
DFF
DFF
DFF
DFF
51 Converter
DFF
DFF
b3
b1
b0
b2
52 4 – bit latch
DFF
DFF
DFF
DFF
A3
A1
A0
A2
53 4 – bit latch
DFF
DFF
DFF
DFF
B3
B1
B0
B2
Parallel output
Signal: 2GHz
Clock: 2GHz
Signal: 2GHz
Clock: 1GHz
Signal: 1GHz
Clock: 1GHz
Signal: 1GHz
Clock: 500MHz
Signal: 500MHz
Clock: 500MHz

Fig. 7

4 – bit latch (n clock) [A3, A2, A1, A0]	Selector (n + 1 clock) [D3, D2, D1, D0]	Control ID
[1, 0, 0, 0]	[A2, A1, A0, B3]	0
[0, 1, 0, 0]	[A1, A0, B3, B2]	1
[0, 0, 1, 0]	[A0, B3, B2, B1]	2
[0, 0, 0, 1]	[B3, B2, B1, B0]	3

Fig. 8

Bit block type	Comparison pattern with selector output [D3, D2, D1, D0]
Synchronization	[0, 0, 0, 1]
Command	[0, 0, 1, 1]
Data	[0, 1, 1, 1]
Wait	[1, 1, 1, 1]

Fig. 9

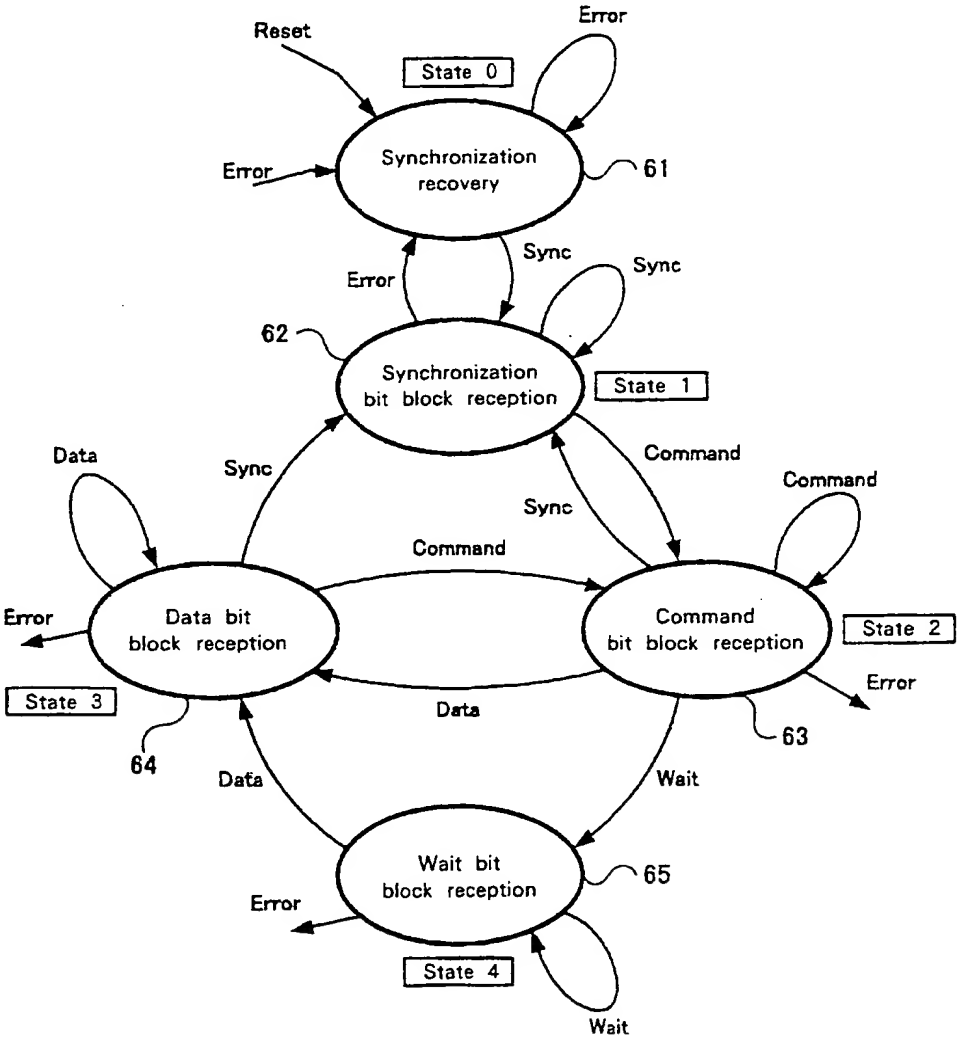

Reset
Error
State 0
Synchronization recovery
61
Error
Error
Sync
Sync
62
Synchronization bit block reception
State 1
Data
Sync
Command
Sync
Command
Command
Error
Data bit block reception
Command bit block reception
State 2
State 3
Error
Data
64
63
Data
Wait
Wait bit block reception
65
Error
State 4
Wait

Fig. 10

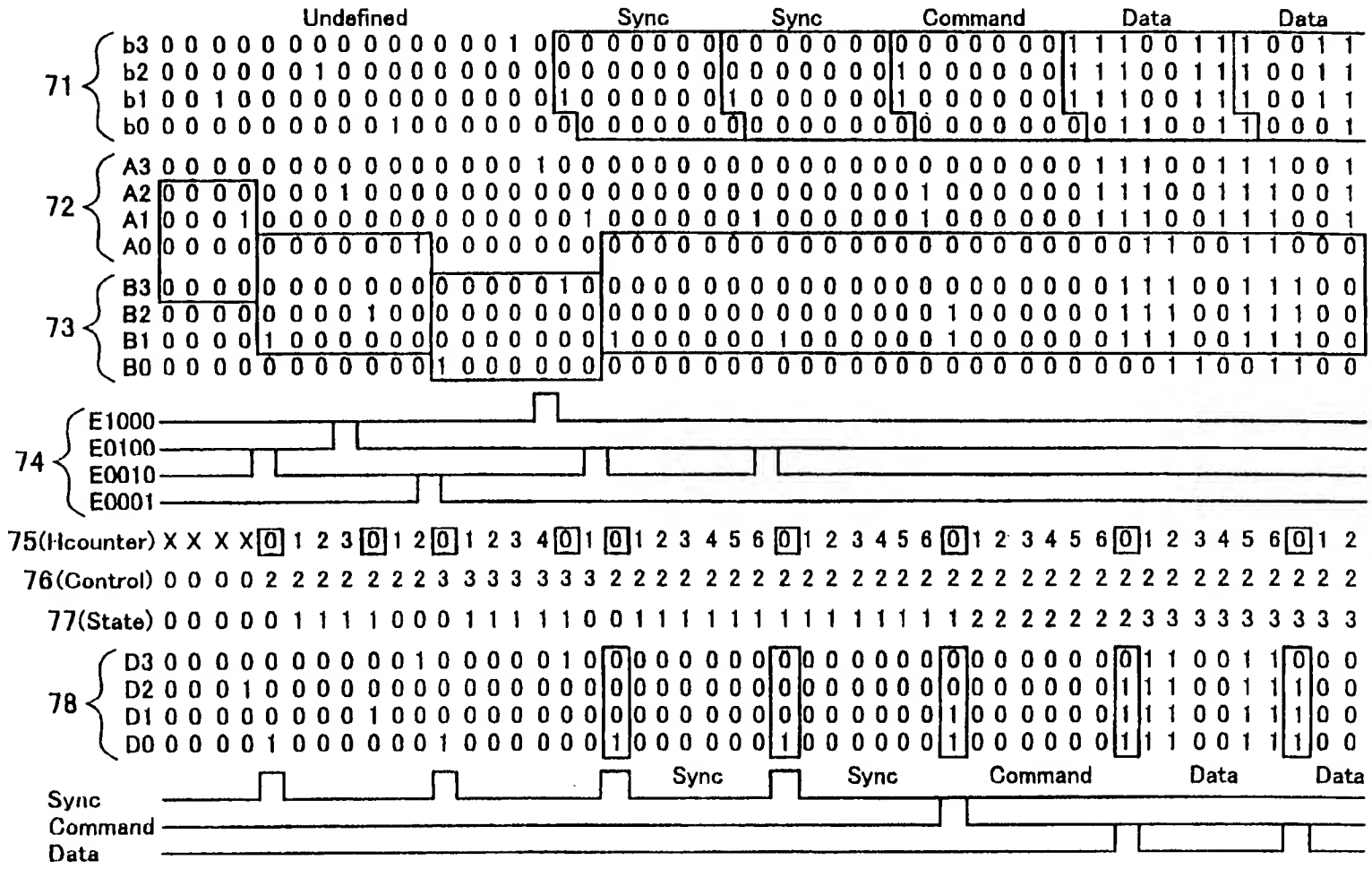

Undefined
Sync
Sync
Command
Data
Data
71
b3
b2
b1
b0
72
A3
A2
A1
A0
73
B3
B2
B1
B0
74
E1000
E0100
E0010
E0001
75(Hcounter)
76(Control)
77(State)
78
D3
D2
D1
D0
Sync
Command
Data

Fig. 11

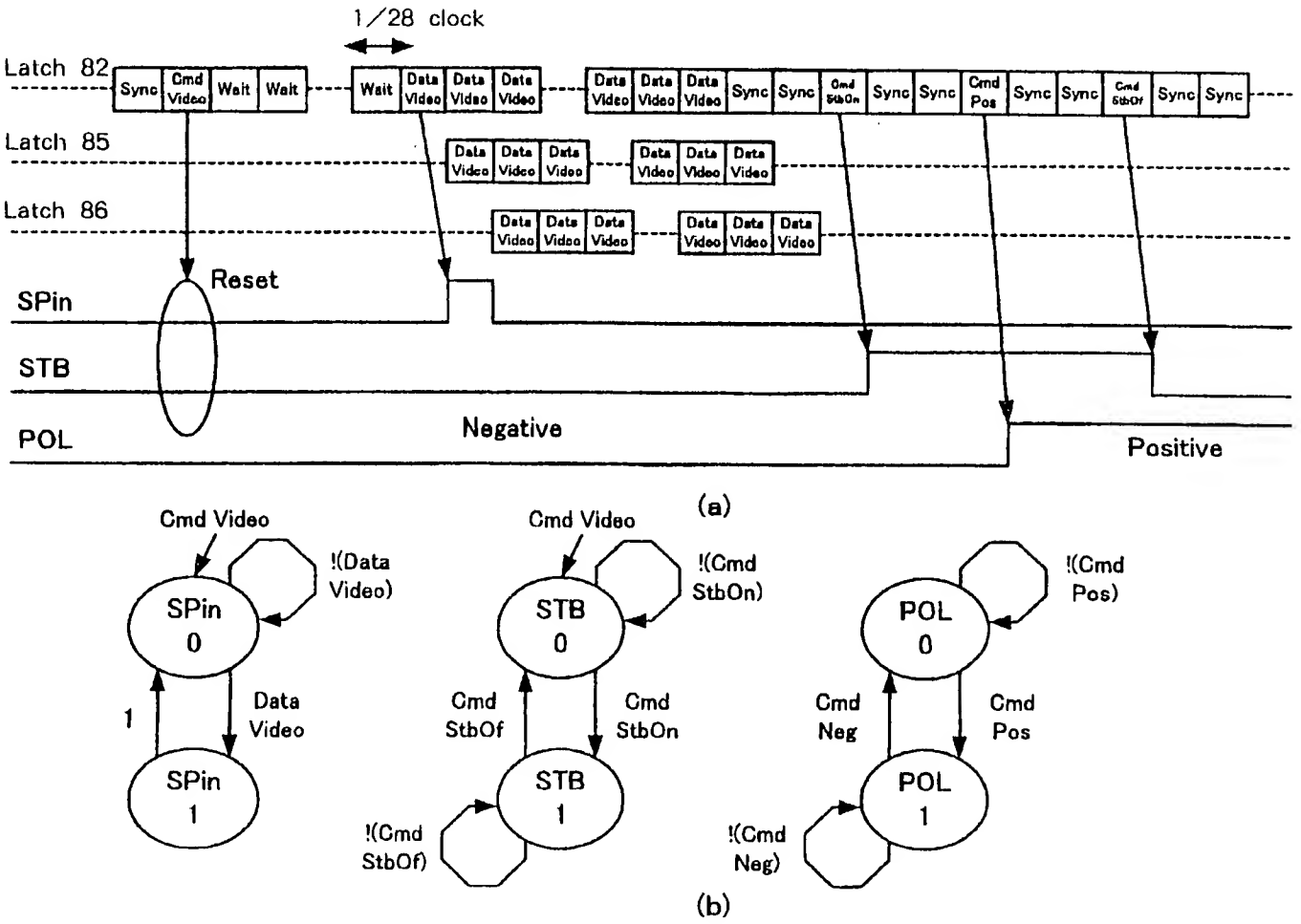

1/28 clock
Latch 82
Latch 85
Latch 86
Sync
Cmd Video
Wait
Data Video
Cmd StbOn
Cmd Pos
Cmd StbOf
Reset
SPin
STB
POL
Negative
Positive
(a)
Cmd Video
!(Data Video)
SPin 0
1
Data Video
SPin 1
Cmd Video
!(Cmd StbOn)
STB 0
Cmd StbOf
Cmd StbOn
STB 1
!(Cmd StbOf)
!(Cmd Pos)
POL 0
Cmd Neg
Cmd Pos
POL 1
!(Cmd Neg)
(b)

Fig. 13

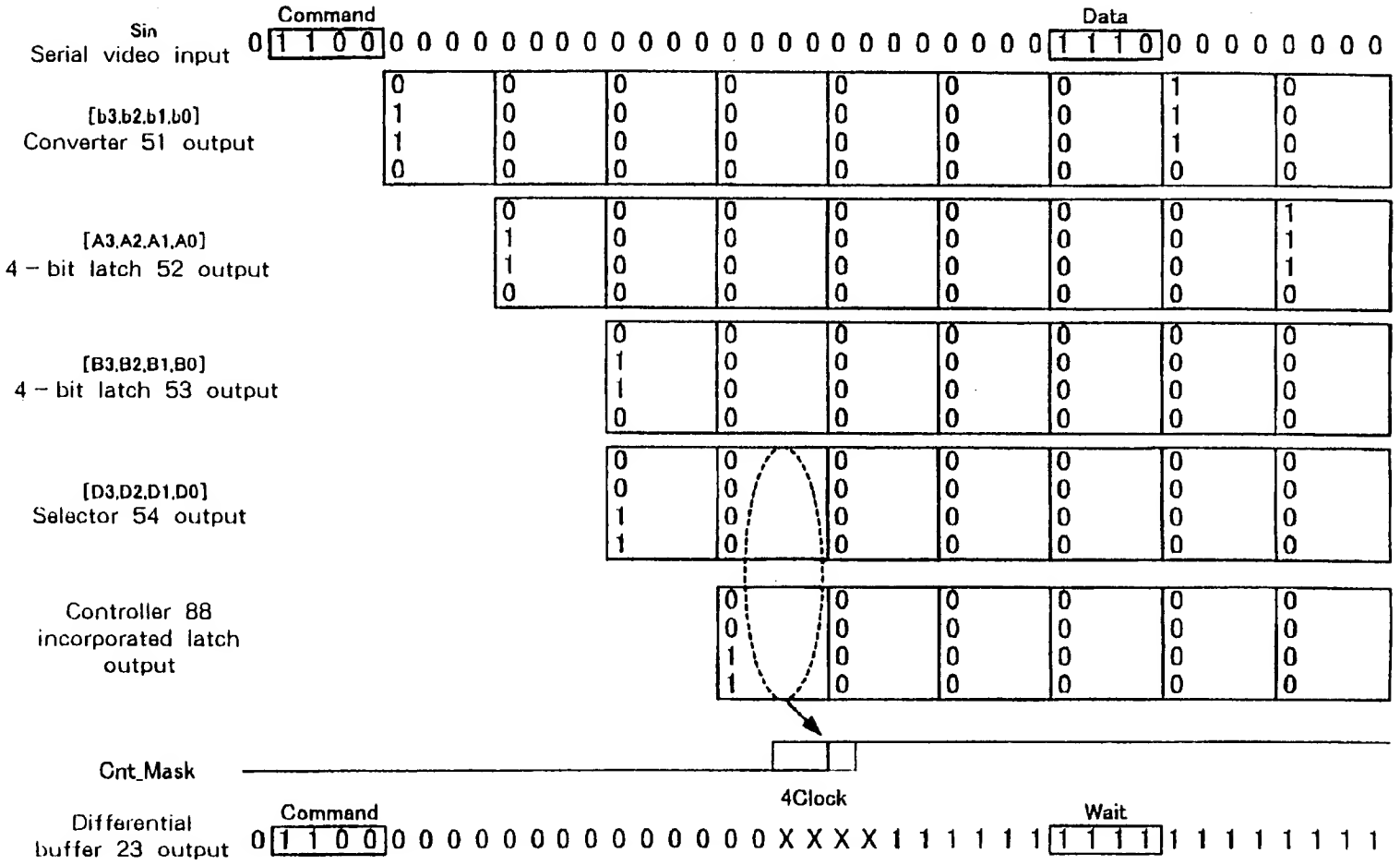

Sin
Serial video input
Command
Data
0 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 0 0 0 0 0 0 0 0
[b3,b2,b1,b0]
Converter 51 output
[A3,A2,A1,A0]
4 – bit latch 52 output
[B3,B2,B1,B0]
4 – bit latch 53 output
[D3,D2,D1,D0]
Selector 54 output
Controller 88
incorporated latch
output
Cnt_Mask
4Clock
Differential
buffer 23 output
Command
Wait
0 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 X X X X 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1

Fig. 14

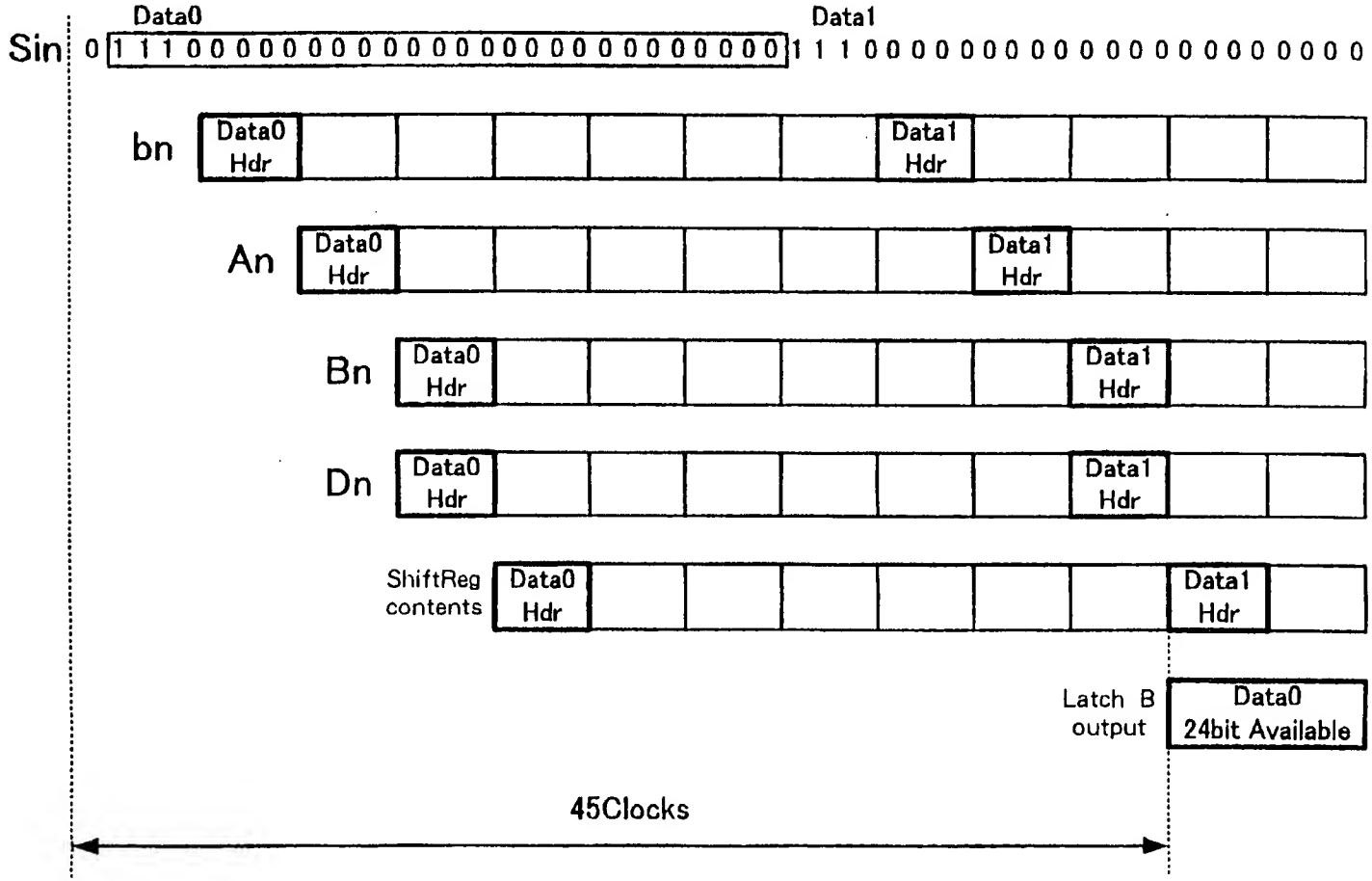

Sin
Data0
Data1
0 1 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
bn
An
Bn
Dn
ShiftReg contents
Data0 Hdr
Data1 Hdr
Latch B output
Data0 24bit Available
45Clocks

Fig. 15

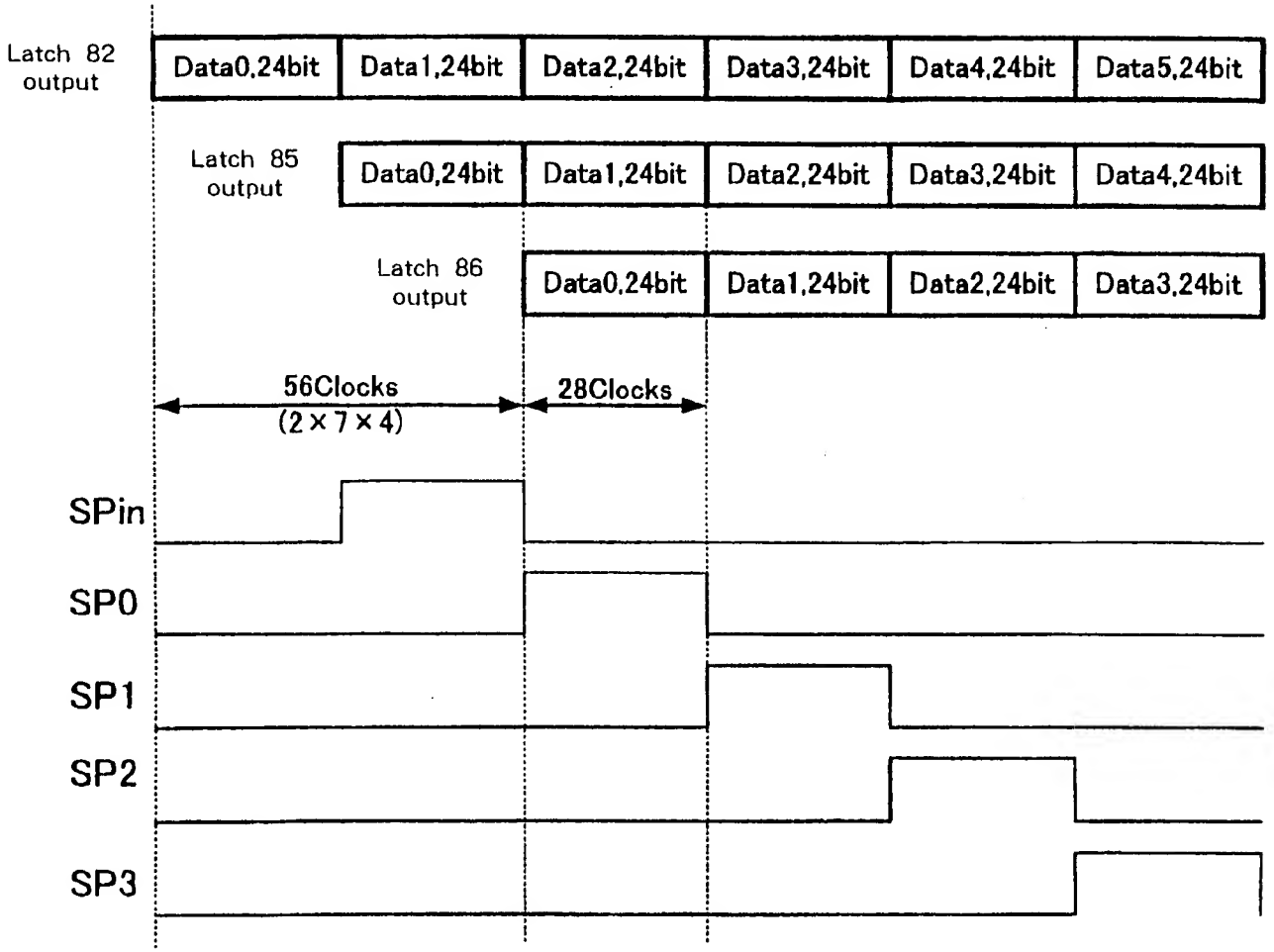

Latch 82 output
Data0,24bit
Data1,24bit
Data2,24bit
Data3,24bit
Data4,24bit
Data5,24bit
Latch 85 output
Data0,24bit
Data1,24bit
Data2,24bit
Data3,24bit
Data4,24bit
Latch 86 output
Data0,24bit
Data1,24bit
Data2,24bit
Data3,24bit
56Clocks
(2×7×4)
28Clocks
SPin
SP0
SP1
SP2
SP3

Fig. 16

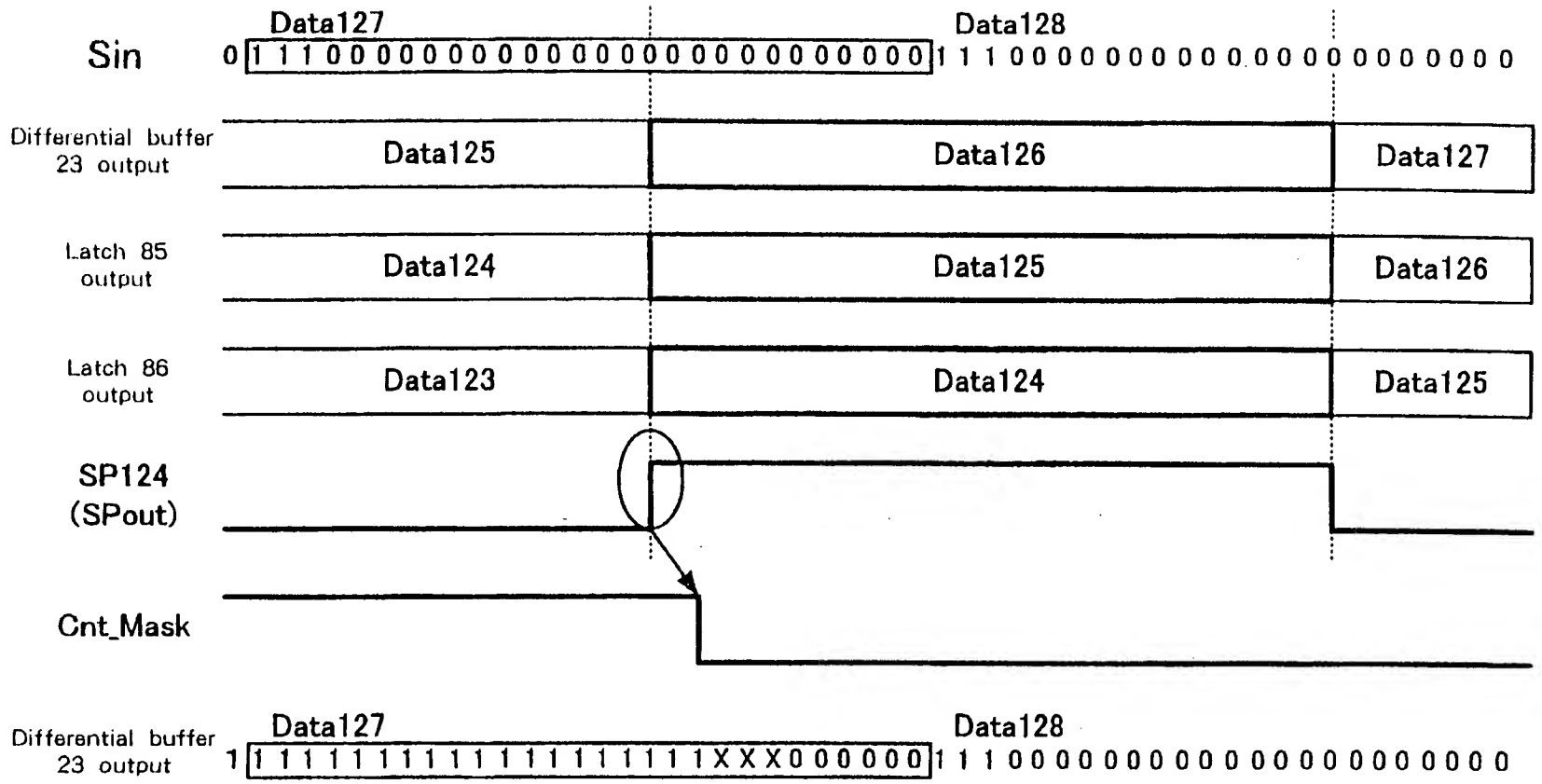

Data127
Data128
Sin
0 1 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Differential buffer 23 output
Data125
Data126
Data127
Latch 85 output
Data124
Data125
Data126
Latch 86 output
Data123
Data124
Data125
SP124 (SPout)
Cnt_Mask
Differential buffer 23 output
Data127
Data128
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 X X X 0 0 0 0 0 0 0 1 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Fig. 17

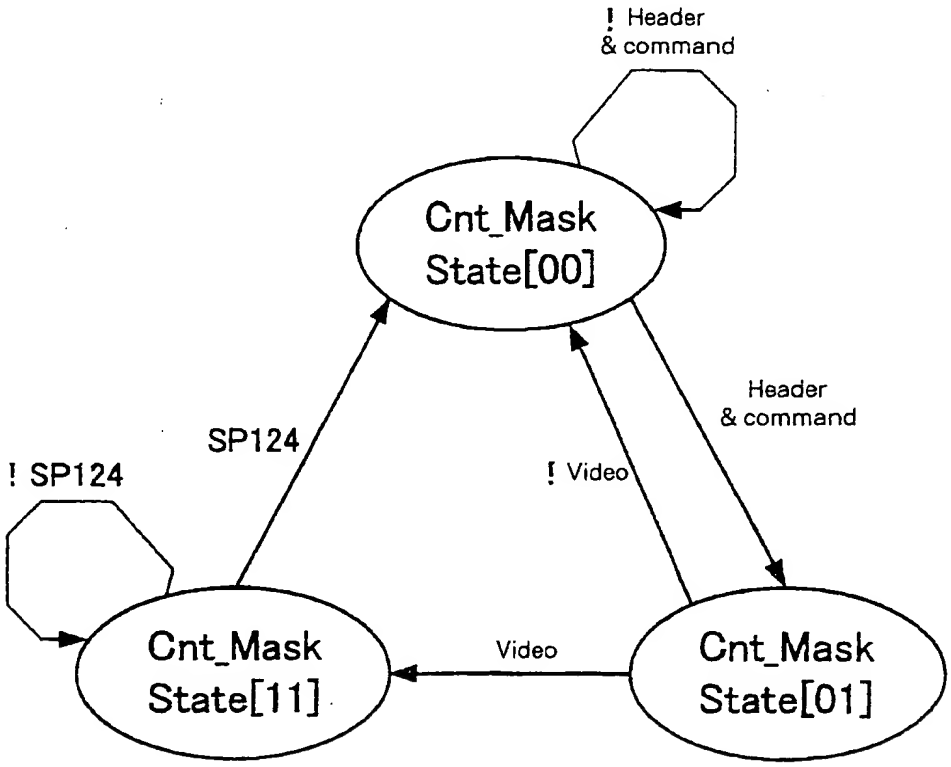
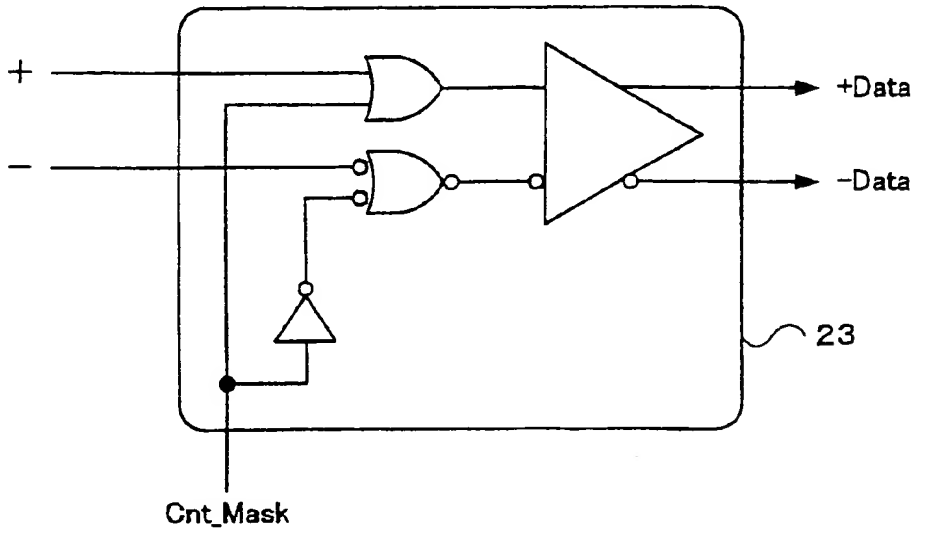

! Header
& command
Cnt_Mask
State[00]
Header
& command
SP124
! SP124
! Video
Cnt_Mask
State[11]
Video
Cnt_Mask
State[01]

Fig. 18



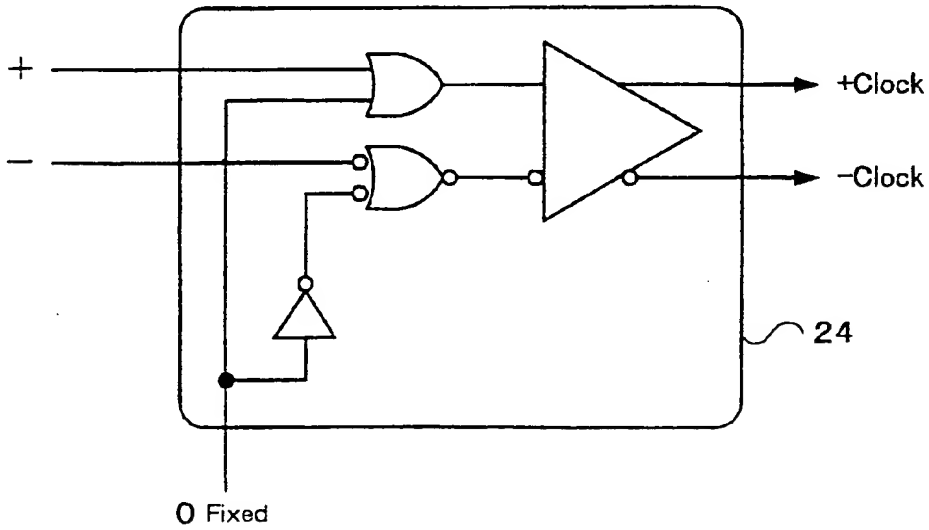


Fig. 19